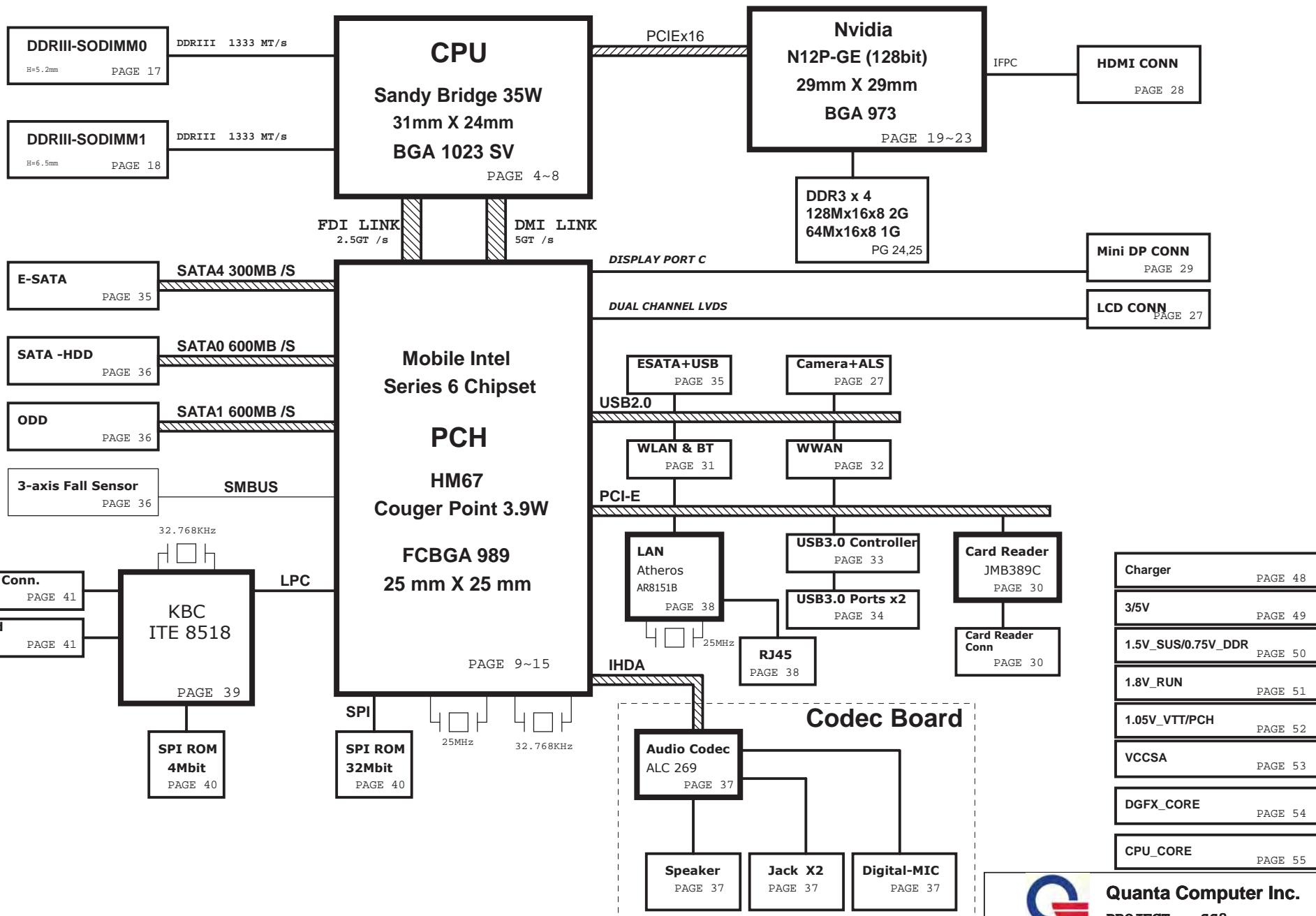


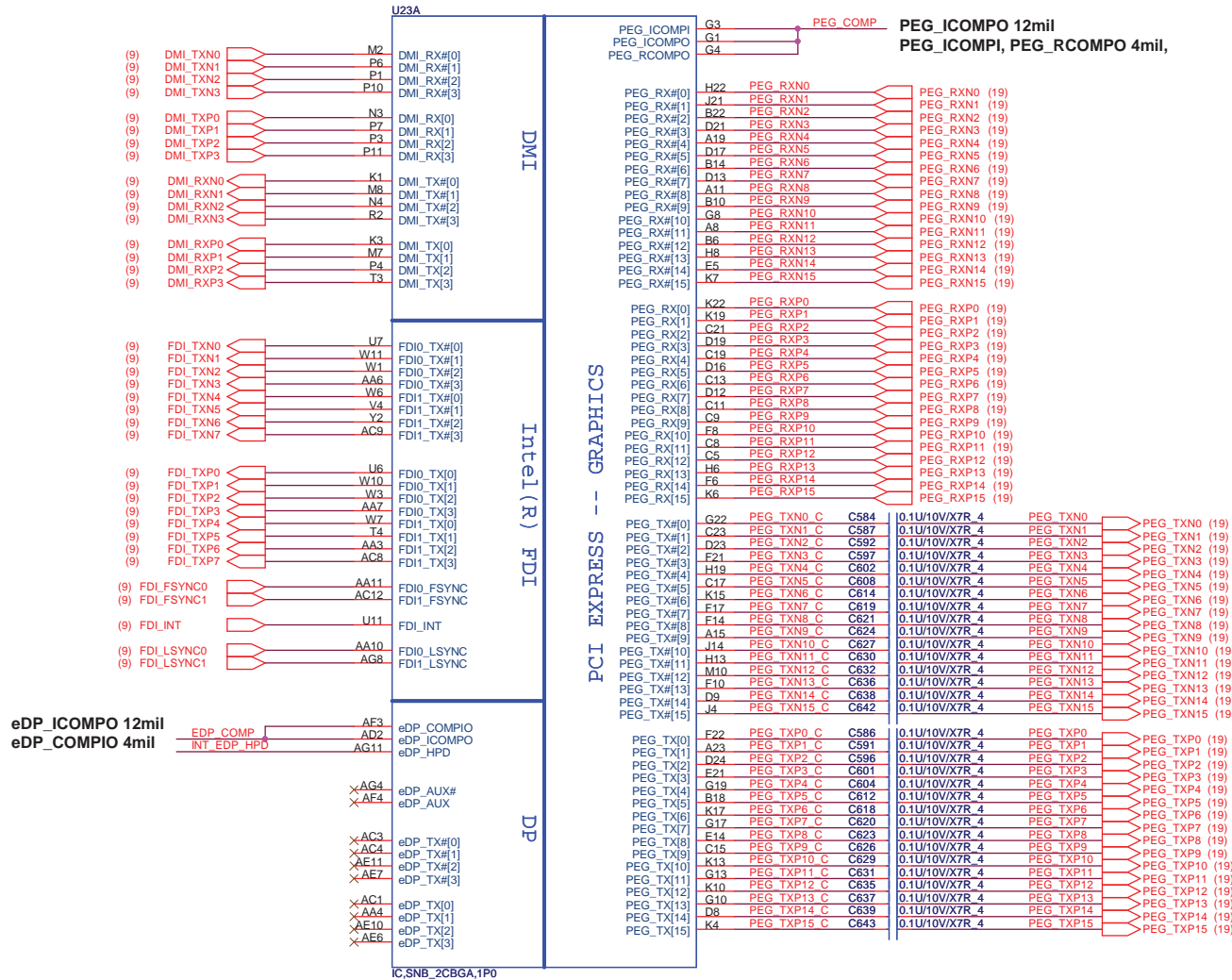
SS8 BLOCK DIAGRAM

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : GND
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : VCC
LAYER 8 : IN4
LAYER 9 : GND
LAYER 10: BOT

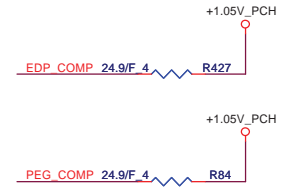


power State					
S0					
S1					
S3					
S4/S5 AC					
S4/S5 DC Only					
AC/DC No Exist					

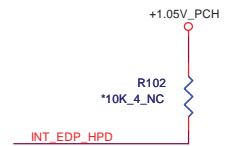
Sandy Bridge Processor (DMI,PEG,FDI)



DP & PEG Compensation

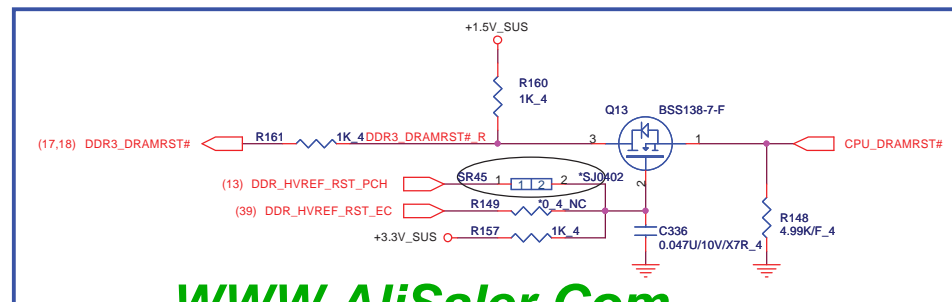


eDP Hot-plug (Disable)



CAD Note: Place PU resistor within 2 inches of CPU

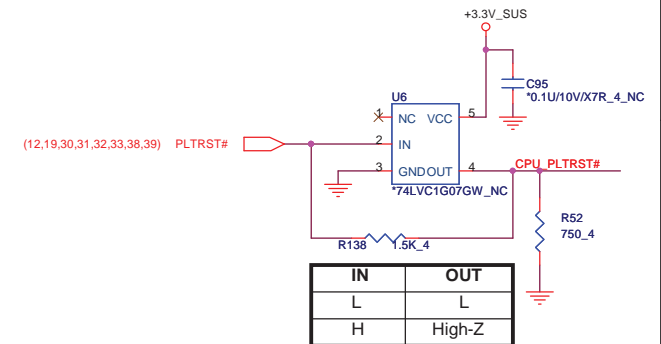
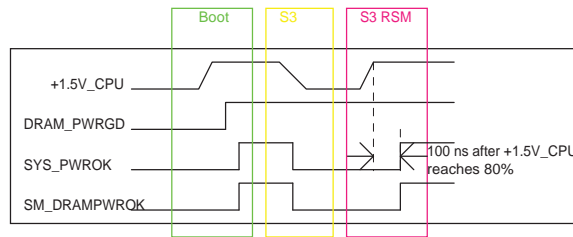
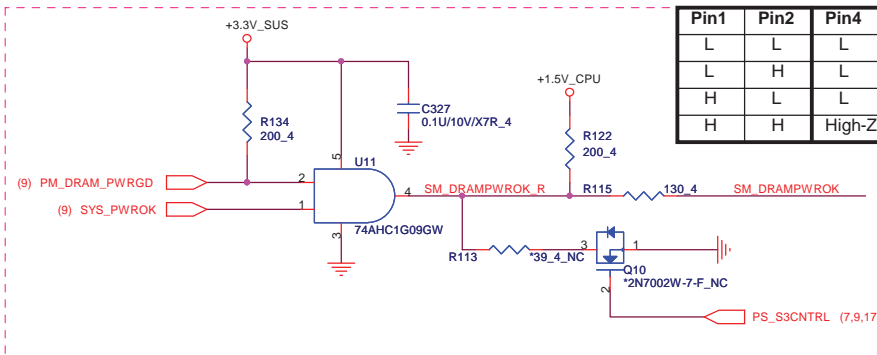
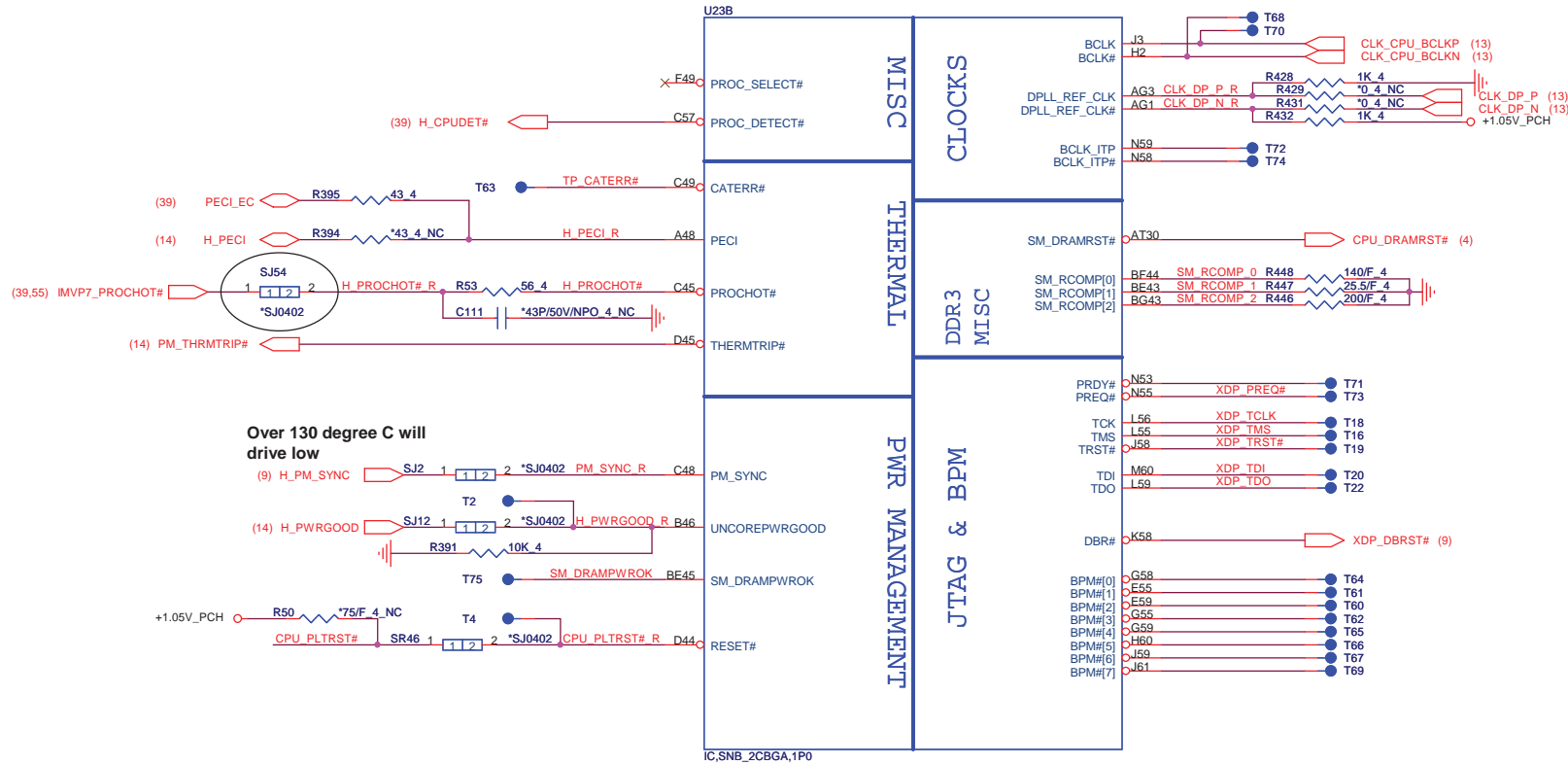
HPDI PU/PD resistor values based on CRB and different to DG



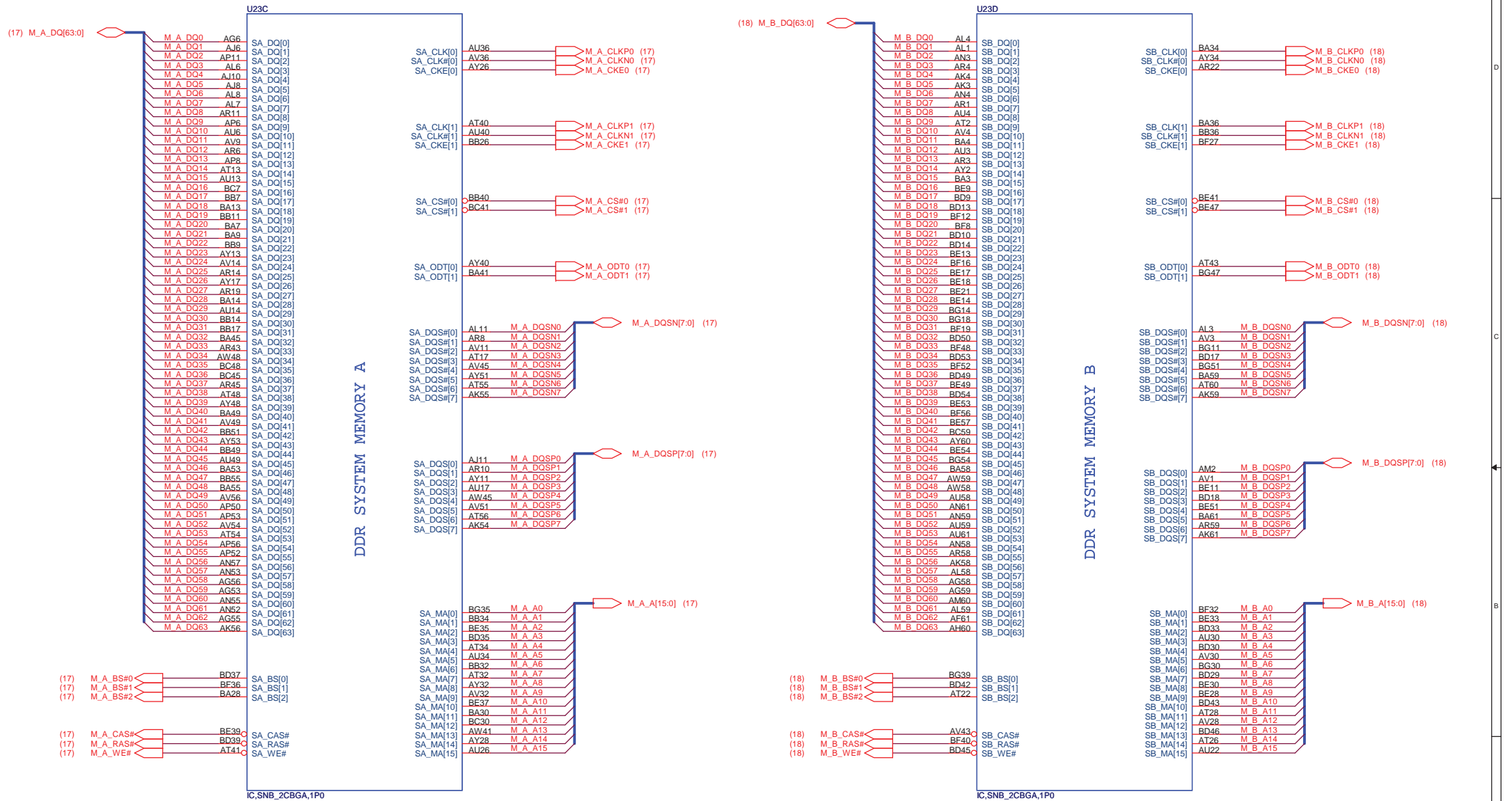
Quanta Computer Inc.
PROJECT : SS8

Size	Document Number	Rev
	Sandy Bridge 1/5	3A
Date:	Monday, January 03, 2011	Sheet 4 of 57

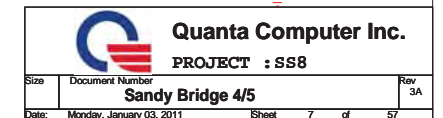
Sandy Bridge Processor (CLK,MISC,JTAG)



Sandy Bridge Processor (DDR3)

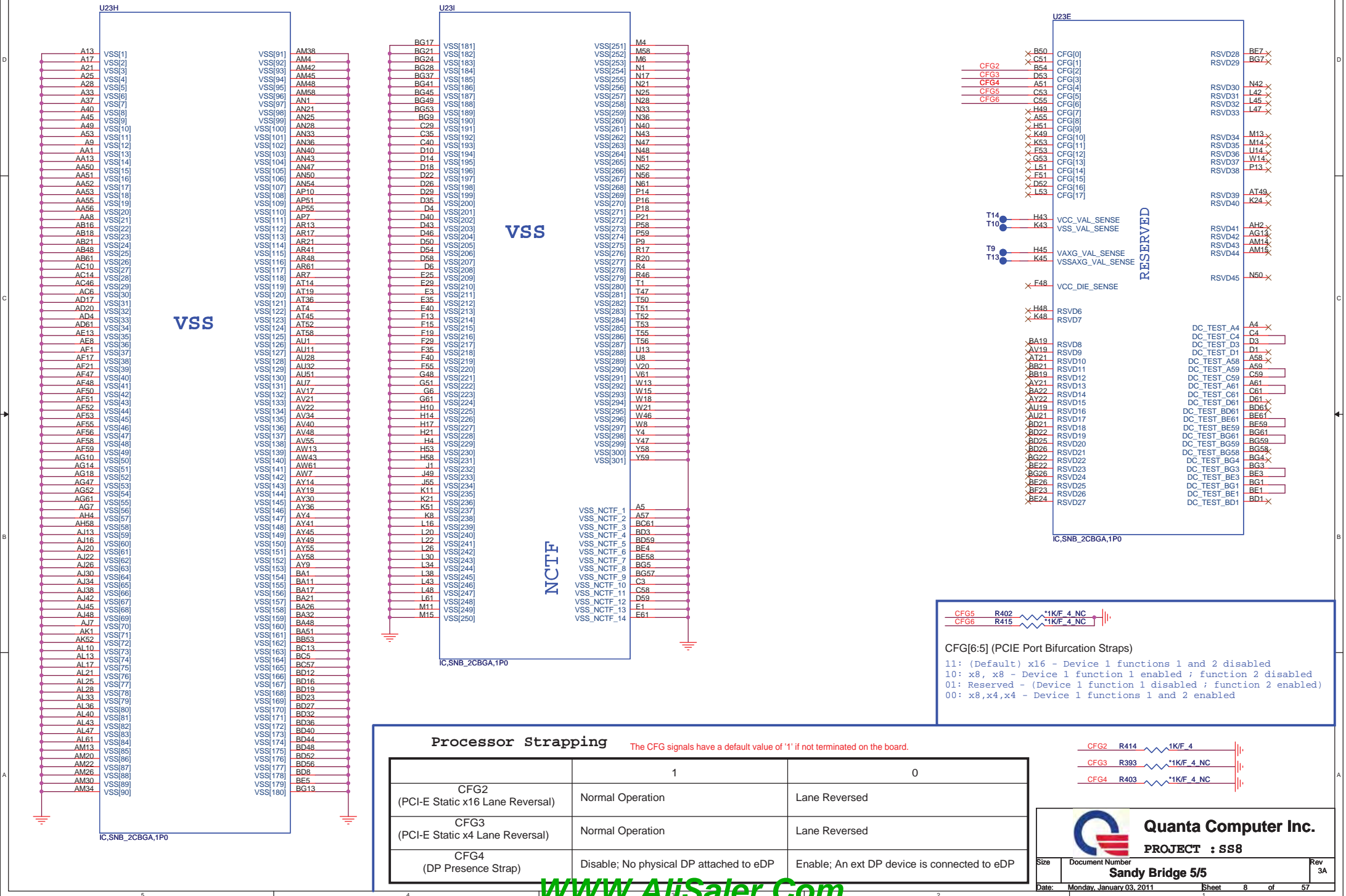


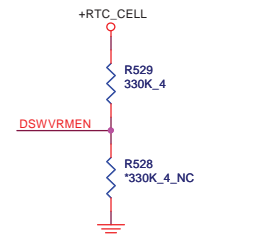
Quanta Computer Inc.
PROJECT : SS8



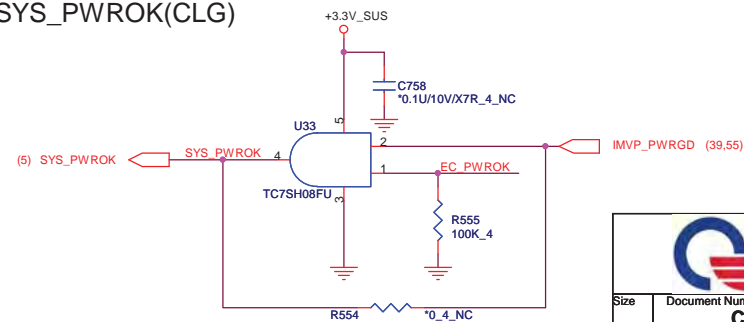
Sandy Bridge Processor (GND)

Sandy Bridge Processor (RESERVED, CFG)



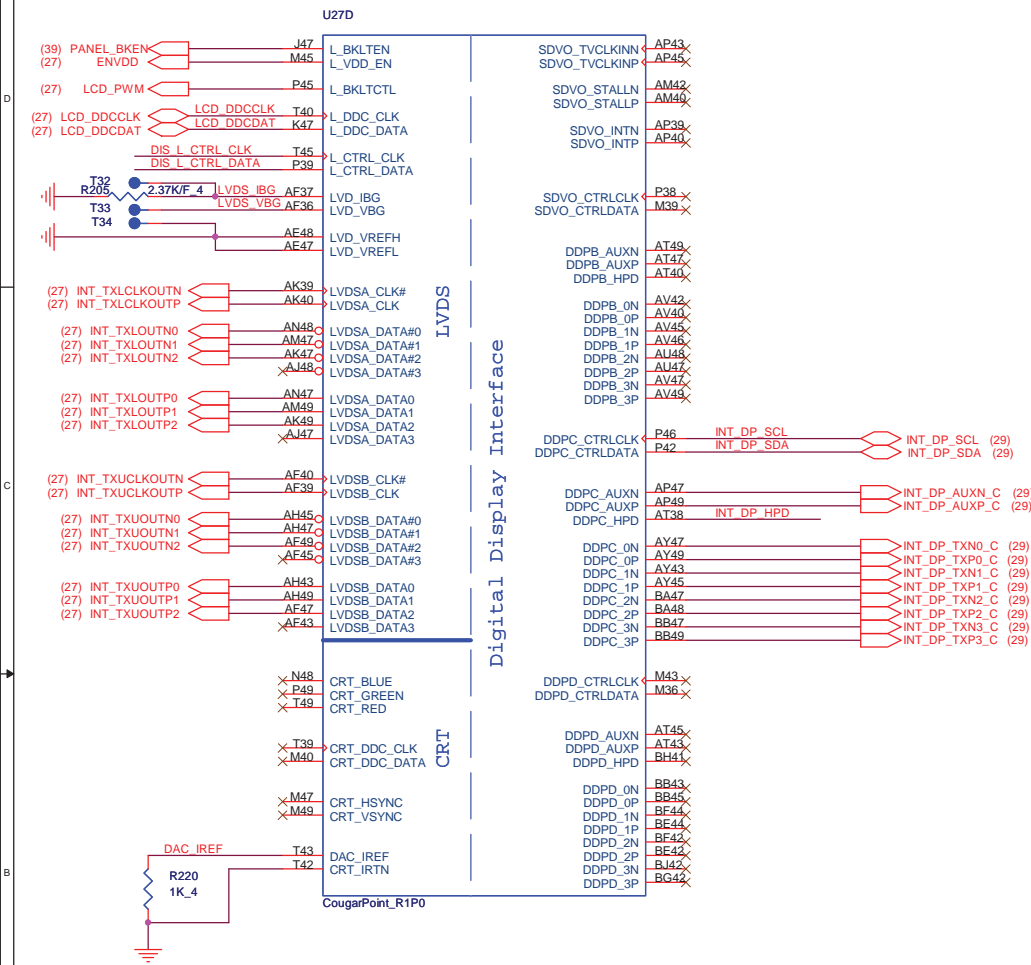


WWW.AliSaler.Com

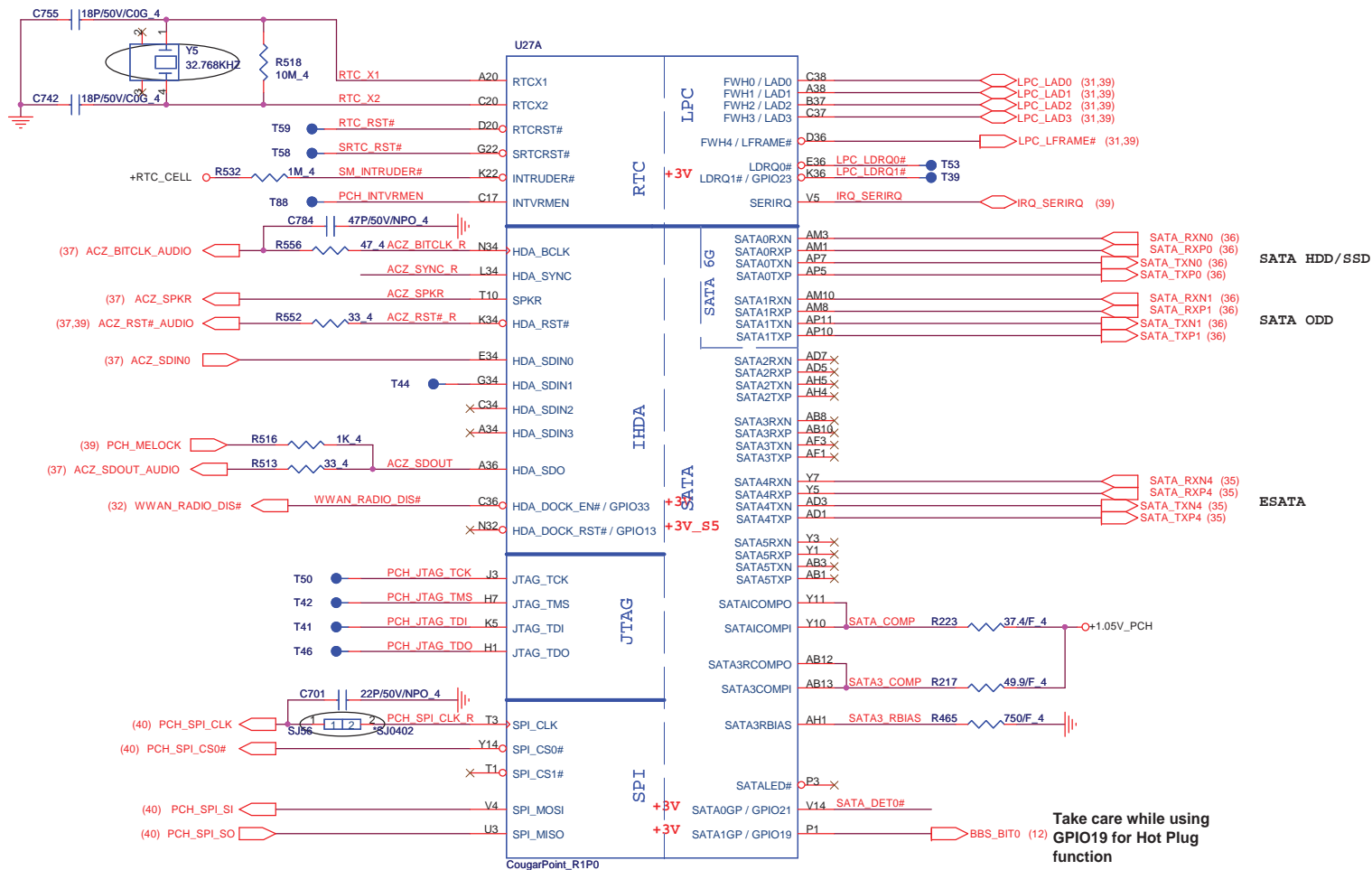


Cougar Point (LVDS,DDI)

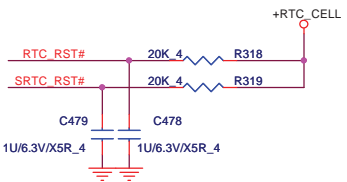
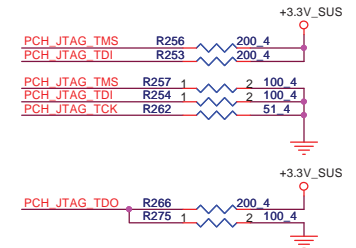
Cougar Point (GND)



Cougar Point (HDA,JTAG,SATA)



PCH JTAG Debug (CLG)



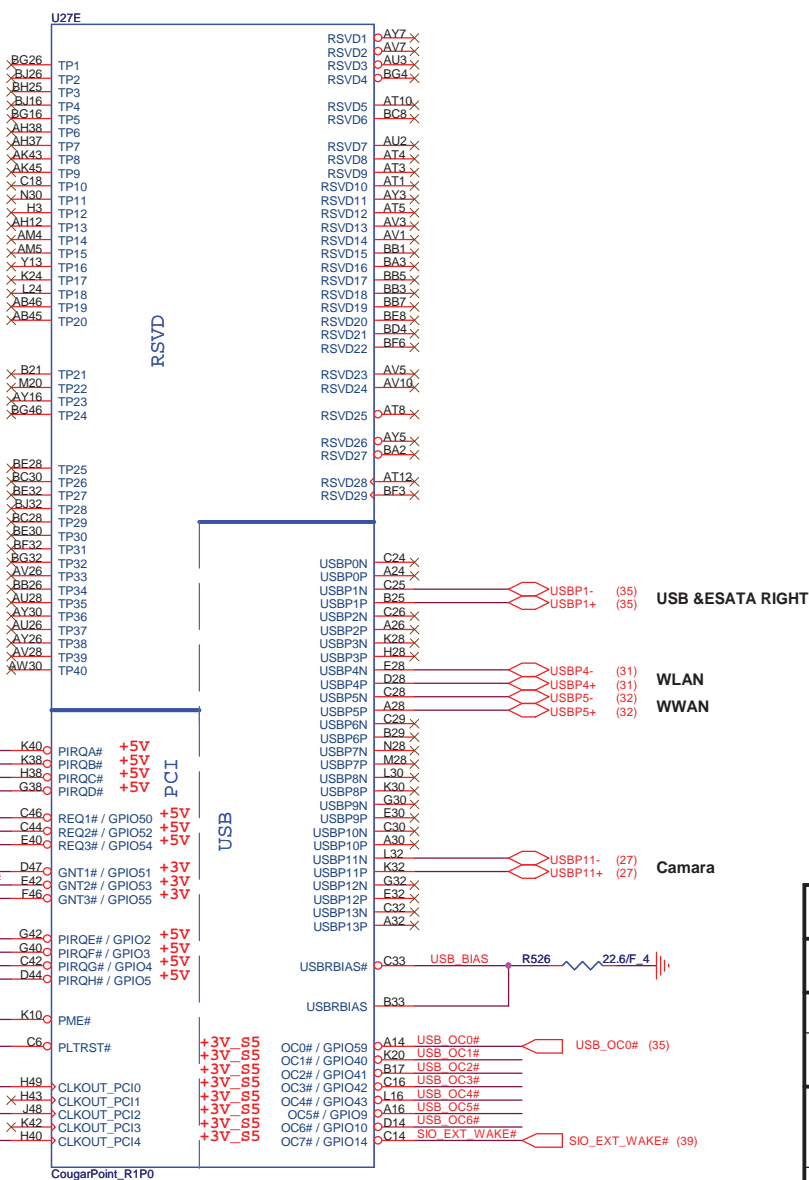
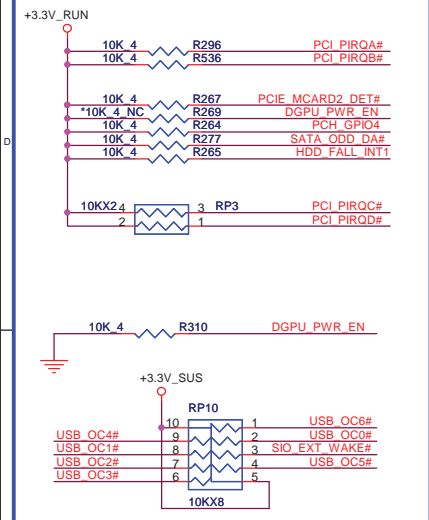
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_RUN R478 1K 4 NC ACZ_SPKR
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS R504 1K 4 NC ACZ_SDOUT
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL R548 330K 4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	(37) ACZ_SYNC_AUDIO R537 33 4 1K 4 R535 +3.3V_SUS

PCI/USBOC Pull-up(CLG)

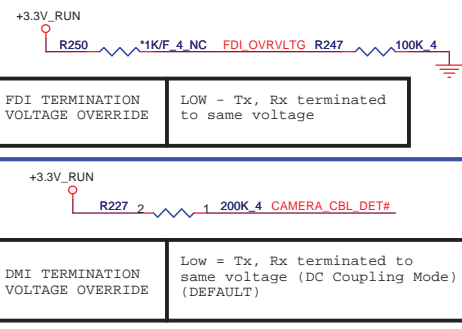
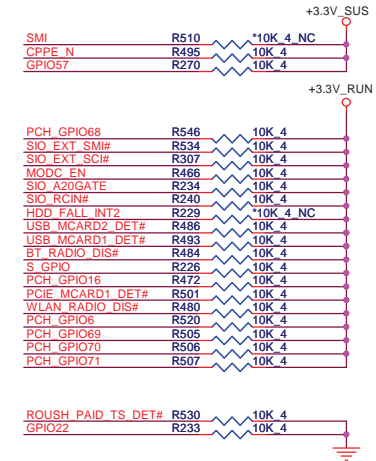
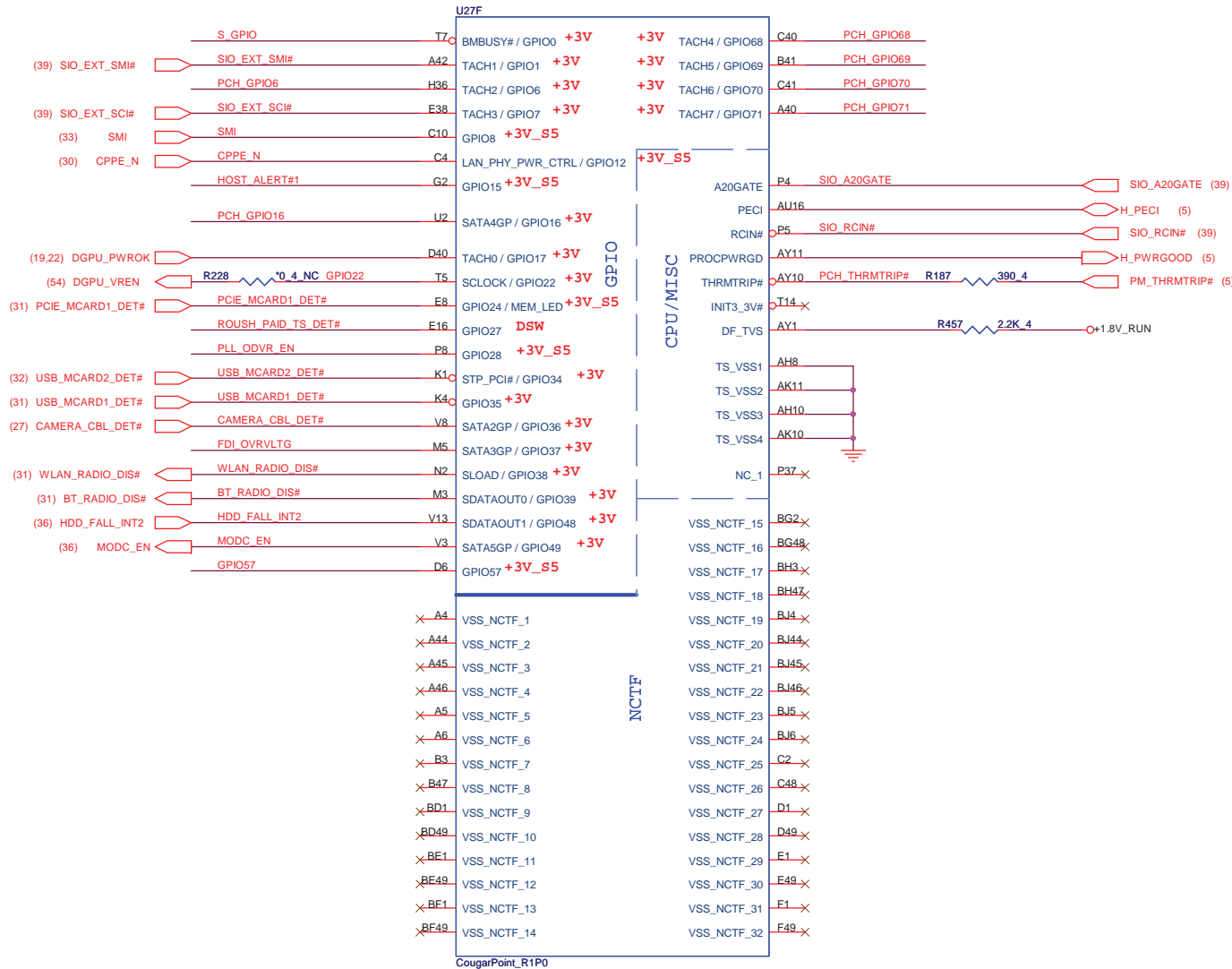
Cougar Point-M (PCI,USB,NVRAM)

PLTRST#(CLG)



Cougar Point (GPIO,VSS_NCTF,RSVD)

GPIO Pull-up/Pull-down(CLG)



Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite	RSMRST#	0 = Disable (Default) 1 = Enable



Quanta Computer Inc.
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COUGAR POINT (POWER)

VccADAC = 1mA(8mils)

VccCORE = 1.14A(50mils)

need 1206?

VccIO = 2.925 A(120mils)

Near to AN16, AP21, AN33

VccVRM(1.5V) = 0.16 A(10mils)

VccDMI = 0.042 A(10mils)

VccCLKDMI = 20mA(8mils)

VccNAND = 190 mA(15mils)

VccSPI = 20mA(8mils)

VccSUS = 10mA(8mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

Cougar Point (POWER)

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VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

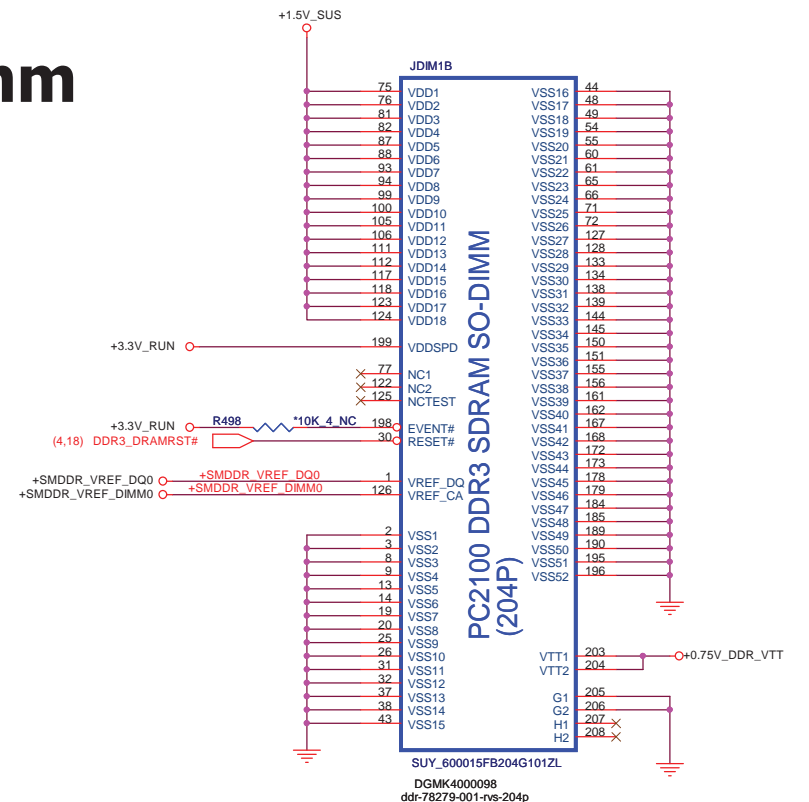
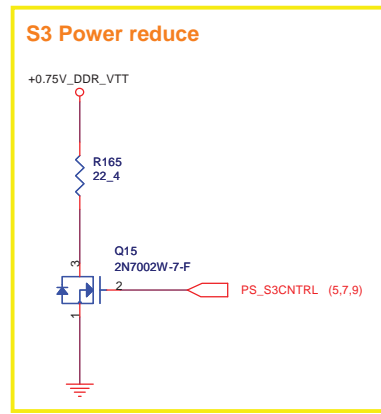
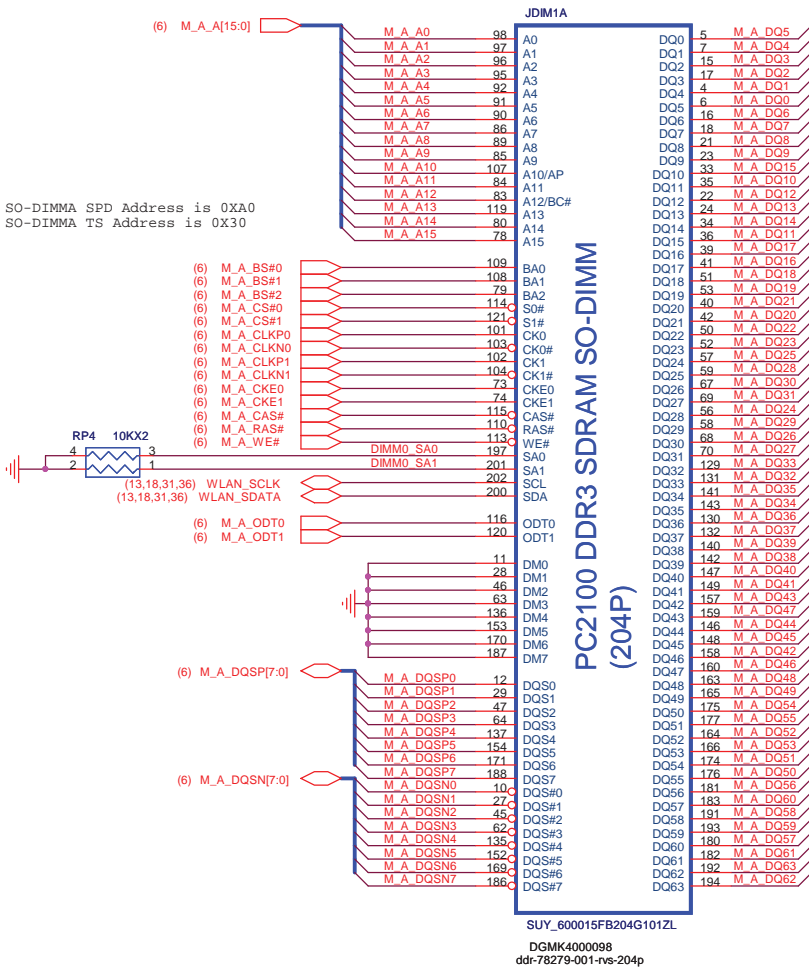
VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

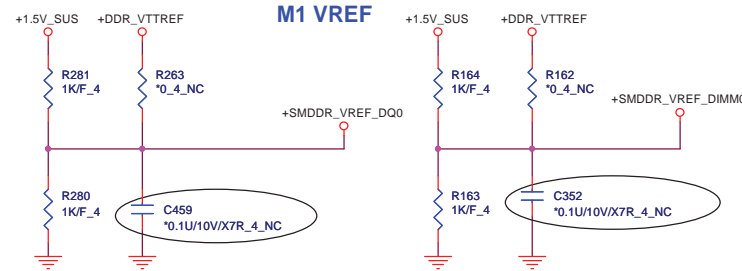
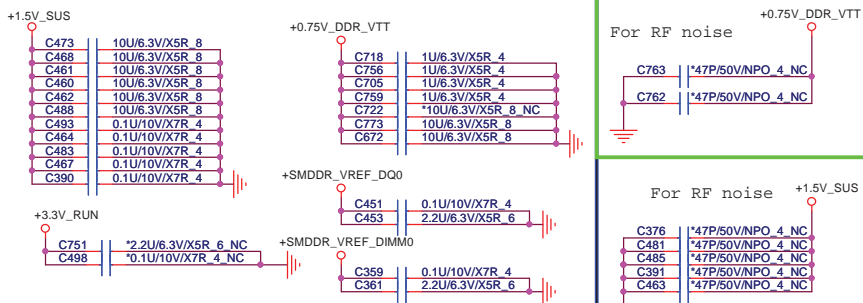
VccSUS3_3 = 119mA(15mils)

VccSUS3_3 = 119mA(15mils)

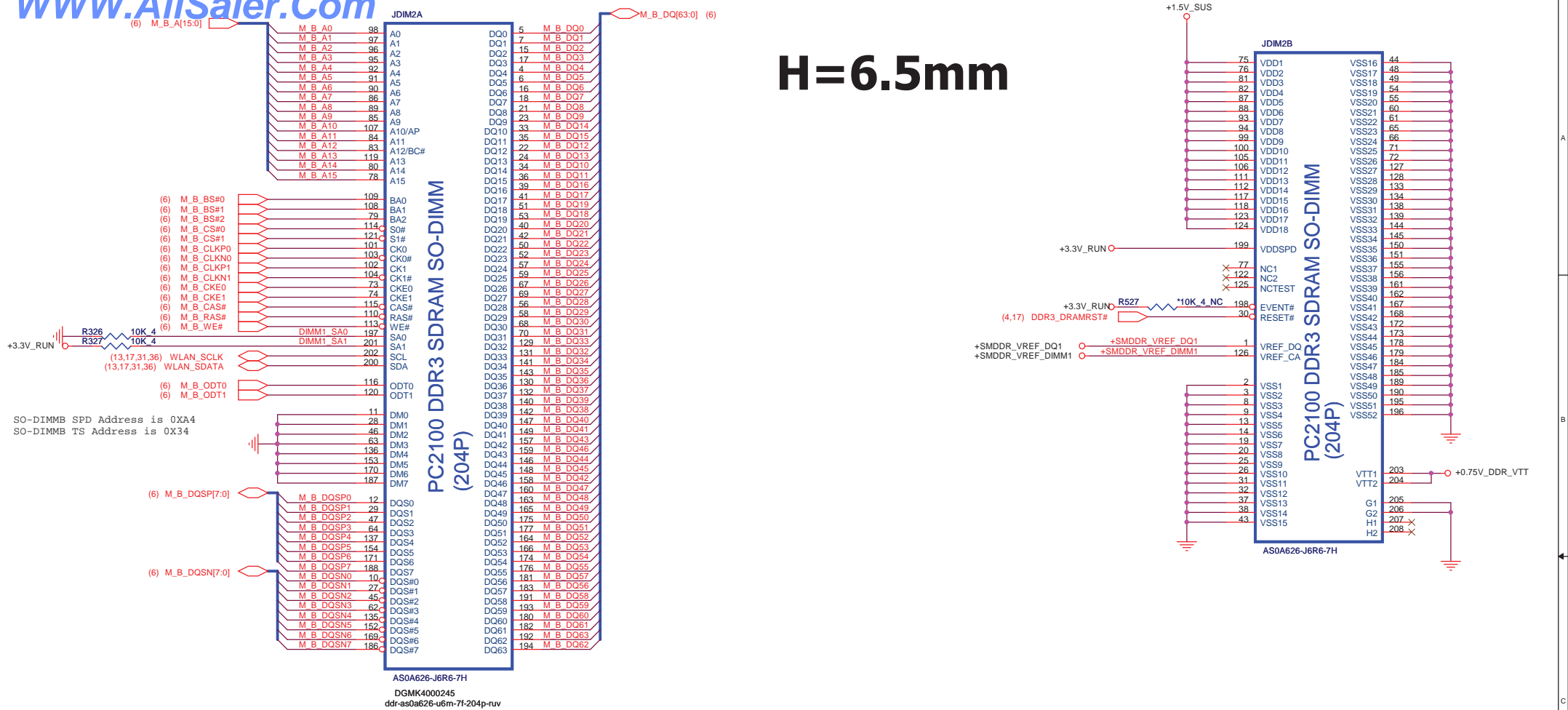
H=5.2mm



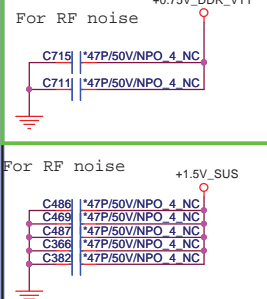
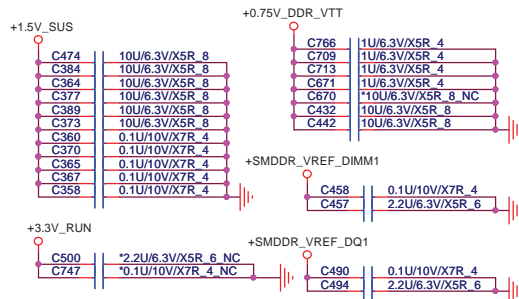
Place these Caps near So-Dimm0.



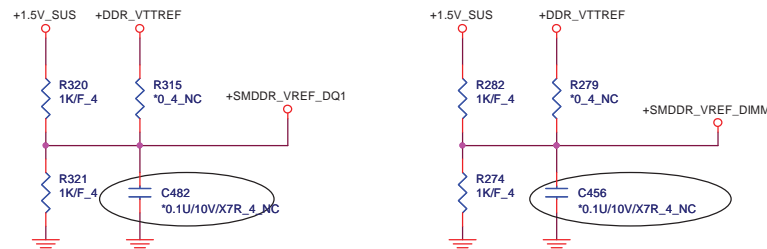
H=6.5mm



Place these Caps near So-Dimm1.



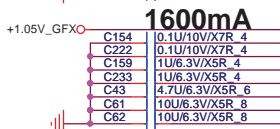
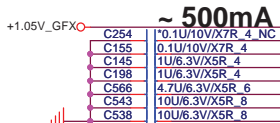
M1 VREF



Quanta Computer Inc.
PROJECT : SS8

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	DDR3 DIMM-1	3A
Date:	Monday, January 03, 2011	Sheet 18 of 57

PEX_IOVDD+PEX_IOVDDQ >2.2A

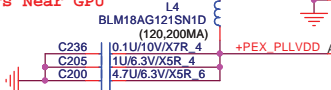


0.1u *4 under GPU
Others Near GPU

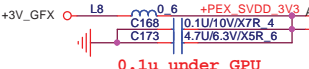
0.1u under GPU
Others Near GPU

**12~16 mils width
120mA**

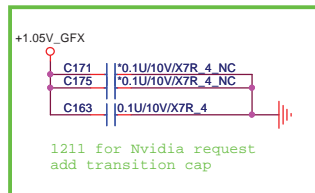
0.1u under GPU
Others Near GPU



120mA 12~16 mils width



0.1u under GPU
Others Near GPU



U22A

N12P-GE

PEX_IOVDD_1
PEX_IOVDD_2
PEX_IOVDD_3
PEX_IOVDD_4
PEX_IOVDD_5

PEX_IOVDDQ_1
PEX_IOVDDQ_2
PEX_IOVDDQ_3
PEX_IOVDDQ_4
PEX_IOVDDQ_5
PEX_IOVDDQ_6
PEX_IOVDDQ_7
PEX_IOVDDQ_8
PEX_IOVDDQ_9
PEX_IOVDDQ_10
PEX_IOVDDQ_11
PEX_IOVDDQ_12
PEX_IOVDDQ_13
PEX_IOVDDQ_14
PEX_IOVDDQ_15
PEX_IOVDDQ_16
PEX_IOVDDQ_17
PEX_IOVDDQ_18
PEX_IOVDDQ_19
PEX_IOVDDQ_20
PEX_IOVDDQ_21
PEX_IOVDDQ_22
PEX_IOVDDQ_23
PEX_IOVDDQ_24
PEX_IOVDDQ_25

PCI EXPRESS

VDD33_1
VDD33_2
VDD33_3
VDD33_4
VDD33_5

VDD_SENSE
NC_9 VDD_SENSE
NC_16 VDD_SENSE

GND_SENSE
NC_10 GND_SENSE
NC_17 GND_SENSE

PEX_PLLVDD

PEX_CAL_PD_VDDQ/PEX_SVDD_3V3
NC_12/PEX_SVDD_3V3

AG20
A2
AB7
AB2
AG6
NC_3
NC_4
NC_5
NC_6
NC_7
AL7
H27
P6
NC_13
NC_15
U7
V6
NC_19

PEX_RX0
PEX_RX0*
PEX_RX1
PEX_RX1*
PEX_RX2
PEX_RX2*
PEX_RX3
PEX_RX3*
PEX_RX4
PEX_RX4*
PEX_RX5
PEX_RX5*
PEX_RX6
PEX_RX6*
PEX_RX7
PEX_RX7*
PEX_RX8
PEX_RX8*
PEX_RX9
PEX_RX9*
PEX_RX10
PEX_RX10*
PEX_RX11
PEX_RX11*
PEX_RX12
PEX_RX12*
PEX_RX13
PEX_RX13*
PEX_RX14
PEX_RX14*
PEX_RX15
PEX_RX15*

PEX_TX0
PEX_TX0*
PEX_TX1
PEX_TX1*
PEX_TX2
PEX_TX2*
PEX_TX3
PEX_TX3*
PEX_TX4
PEX_TX4*
PEX_TX5
PEX_TX5*
PEX_TX6
PEX_TX6*
PEX_TX7
PEX_TX7*
PEX_TX8
PEX_TX8*
PEX_TX9
PEX_TX9*
PEX_TX10
PEX_TX10*
PEX_TX11
PEX_TX11*
PEX_TX12
PEX_TX12*
PEX_TX13
PEX_TX13*
PEX_TX14
PEX_TX14*
PEX_TX15
PEX_TX15*

AL17 PEG_RXP15 C C221 0.1U/10V/X7R 4
AM17 PEG_RXN15 C C206 0.1U/10V/X7R 4
AM18 PEG_RXP14 C C186 0.1U/10V/X7R 4
AM19 PEG_RXN14 C C174 0.1U/10V/X7R 4
AL18 PEG_RXP13 C C198 0.1U/10V/X7R 4
AL20 PEG_RXP12 C C167 0.1U/10V/X7R 4
AM20 PEG_RXN12 C C162 0.1U/10V/X7R 4
AM21 PEG_RXP11 C C157 0.1U/10V/X7R 4
AM22 PEG_RXN11 C C150 0.1U/10V/X7R 4
AL22 PEG_RXP10 C C172 0.1U/10V/X7R 4
AL22 PEG_RXN10 C C164 0.1U/10V/X7R 4
AL23 PEG_RXP9 C C149 0.1U/10V/X7R 4
AM23 PEG_RXN9 C C144 0.1U/10V/X7R 4
AM24 PEG_RXP8 C C140 0.1U/10V/X7R 4
AM25 PEG_RXN8 C C130 0.1U/10V/X7R 4
AL25 PEG_RXP7 C C127 0.1U/10V/X7R 4
AK25 PEG_RXN7 C C125 0.1U/10V/X7R 4
AL26 PEG_RXP6 C C119 0.1U/10V/X7R 4
AM26 PEG_RXN6 C C114 0.1U/10V/X7R 4
AM27 PEG_RXP5 C C112 0.1U/10V/X7R 4
AM28 PEG_RXN5 C C109 0.1U/10V/X7R 4
AL28 PEG_RXP4 C C107 0.1U/10V/X7R 4
AK28 PEG_RXN4 C C102 0.1U/10V/X7R 4
AL29 PEG_RXP3 C C100 0.1U/10V/X7R 4
AM29 PEG_RXN3 C C97 0.1U/10V/X7R 4
AM30 PEG_RXP2 C C96 0.1U/10V/X7R 4
AM31 PEG_RXN2 C C92 0.1U/10V/X7R 4
AM32 PEG_RXP1 C C91 0.1U/10V/X7R 4
AM33 PEG_RXN1 C C88 0.1U/10V/X7R 4
AN32 PEG_RXP0 C C89 0.1U/10V/X7R 4
AP32 PEG_RXN0 C C84 0.1U/10V/X7R 4

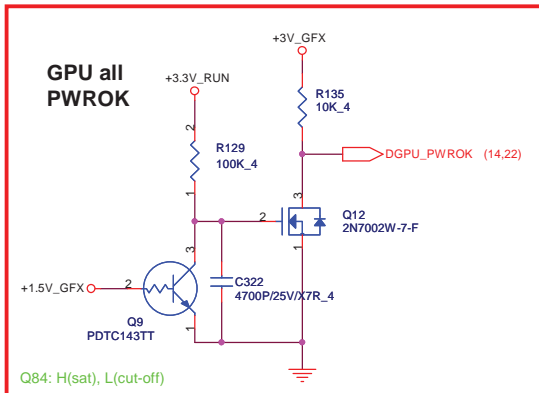
PEX_REFCLK
PEX_REFCLK*

PEX_RST#

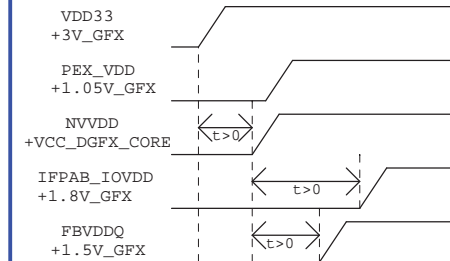
PEX_CLKREQ#

PEX_TERM

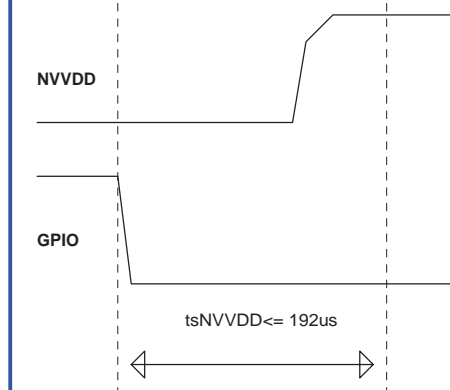
TESTMODE



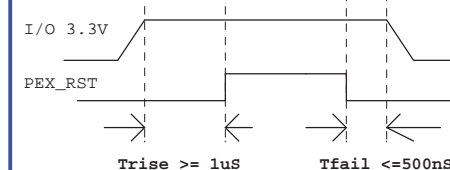
Power up sequence



NB9M: VGACORE +0.90V (Normal) , +1.09V
NVVDD Maximum Settling Time

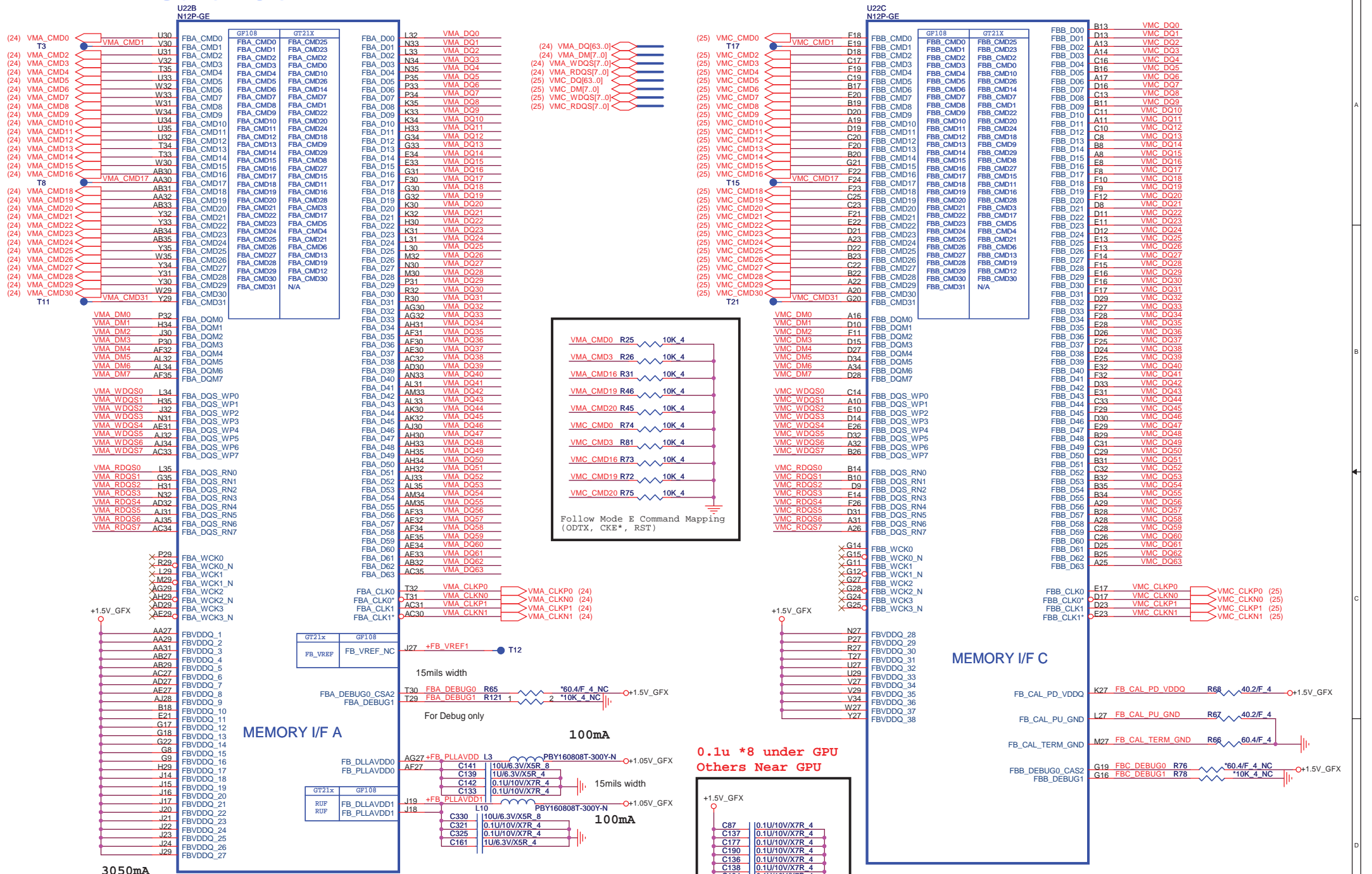


PEX_RST timing



Quanta Computer Inc.

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Default: N12P-GE

The left diagram shows the connection of the 3V_GFX pin to the ROM chip select and clock inputs. The 3V_GFX pin is connected to the top of a 4.99K pull-up resistor (R441) and the top of a 4.99K pull-down resistor (R155). The bottom of R155 is connected to ground. The bottom of R441 is connected to the ROM_SI input. The ROM_SCLK input is connected to the top of a 35.7K pull-down resistor (R436) and the top of a 15K pull-down resistor (R154). The bottom of R436 is connected to ground. The bottom of R154 is connected to the ROM_SCLK input.

The right diagram shows the connection of the 3V_GFX pin to the STRAP inputs. The 3V_GFX pin is connected to the top of a 45.3K pull-up resistor (R141) and the top of a 35.7K pull-down resistor (R152). The bottom of R152 is connected to ground. The bottom of R141 is connected to the STRAP0 input. The STRAP1 and STRAP2 inputs are connected to the top of a 35.7K pull-down resistor (R151) and the top of a 30.1K pull-down resistor (R123). The bottom of R151 is connected to ground. The bottom of R123 is connected to the STRAP2 input.

10K1/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]	30.1K/F 4: CS33012FB18 [RES CHIP 30.1K 1/16W +1% (0402)]
4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1% (0402)]	35.7K/F 4: CS33572FB13 [RES CHIP 35.7K 1/16W +1% (0402)]
15K1/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]	45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1% (0402)]
20K1/F 4: CS32002FB29 RES CHIP 20K 1/16W +1% (0402)	

Default: Hynix VRAM 2G (0110) [VRAM Configuration Table](#)

The diagram shows the timing of various signals relative to a 3V_GF supply. The signals are connected to a common bus through resistors (R98, R103, R133, R444, R144, R166, R180, R445, R143, R100, R94, R439) and a 10K 4 NC component. The signals are:

- JTAG_TMS (R98, 10K 4 NC)
- JTAG_TDI (R103, 10K 4 NC)
- VGA_OVT# (R133, 10K 4)
- DGPU_VID1 (R444, 10K 4 NC)
- DGPU_VID2 (R144, 10K 4)
- VGA_ALERT (R166, 10K 4)
- VGA_PWR_LEVEL (R180, 10K 4)
- DGPU_VID1 (R445, 10K 4)
- DGPU_VID2 (R143, 10K 4 NC)
- JTAG_TCK (R100, 10K 4 NC)
- JTAG_TRST# (R94, 10K 4)
- EXT_HDMI_HPD (R439, 100K 4)

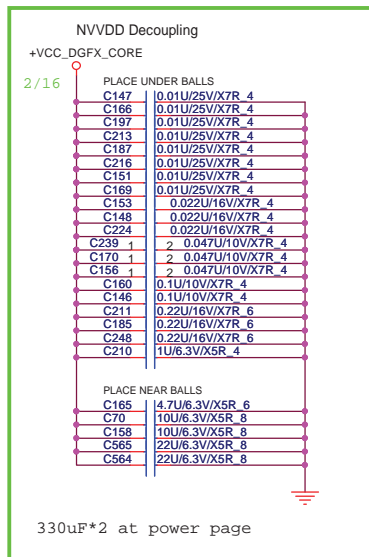
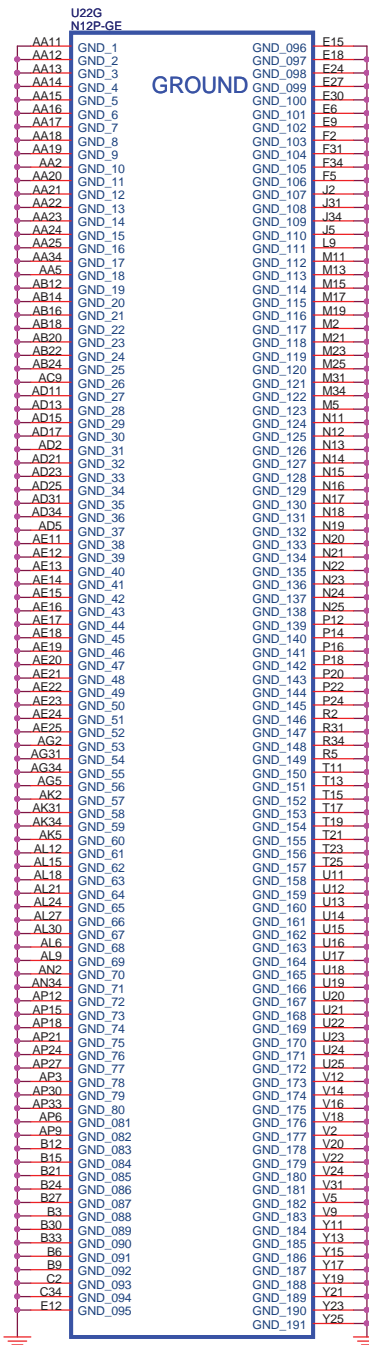
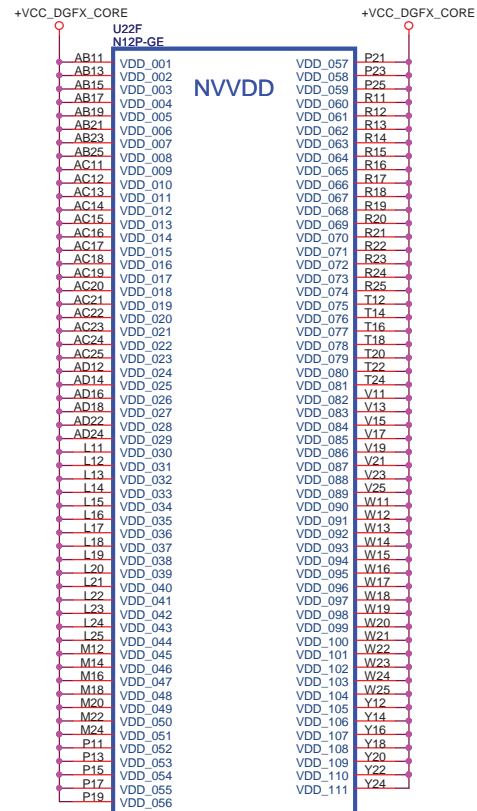
GPI/O	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVD0 VID0
6	OUT	N/A	NVVD1 VID1
7	OUT	N/A	NVVD2 VID2 ^{11/13}
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL ^{11/13}
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL



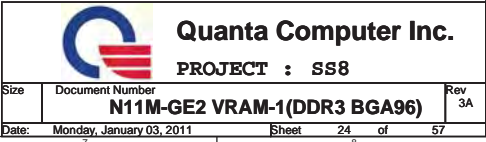
Quanta Computer Inc.

PROJECT : SS8

Size	Document Number	Rev
	N12P-GE (GPIO&STRAPS) 4/5	3A
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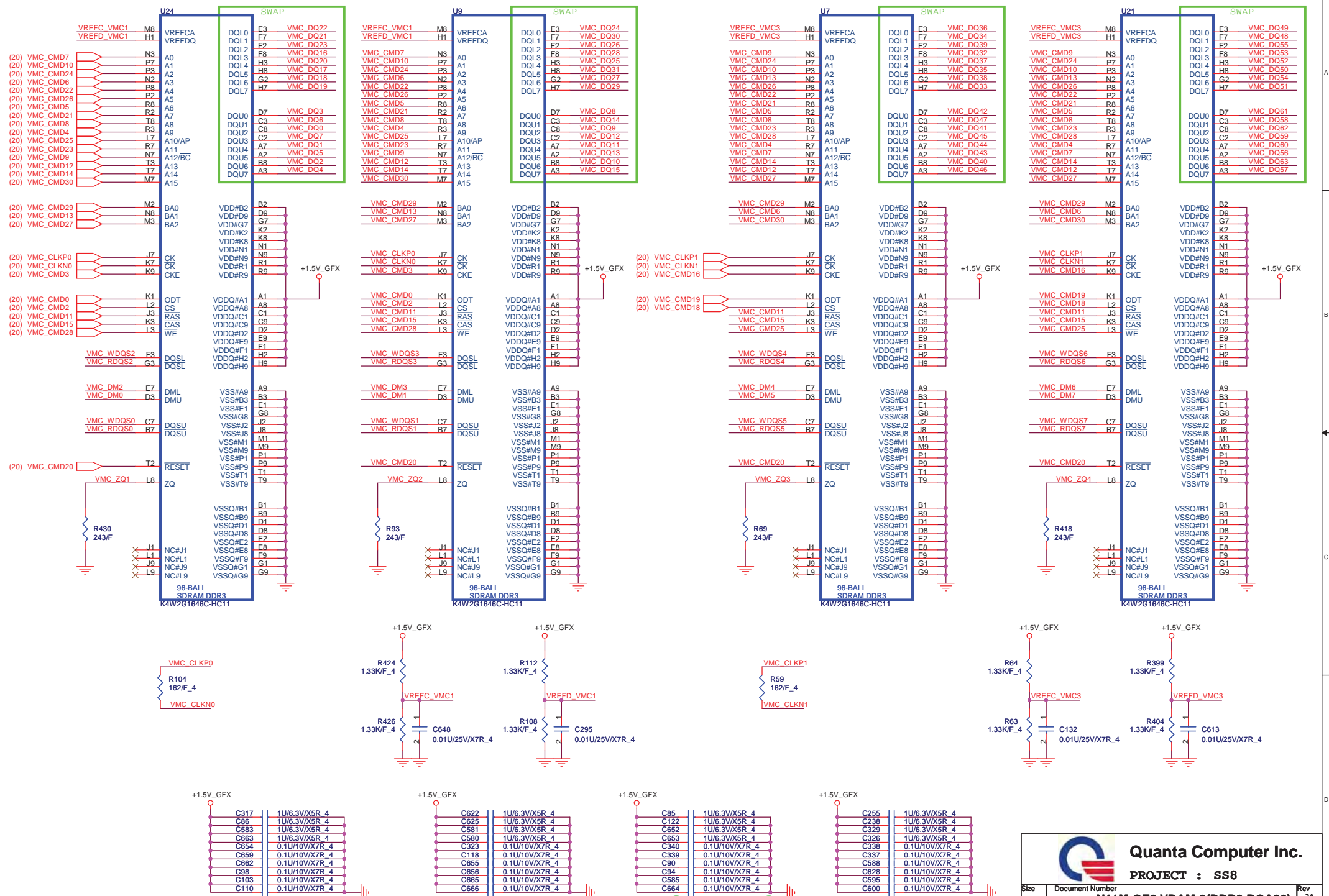


WWW.AliSaler.Com

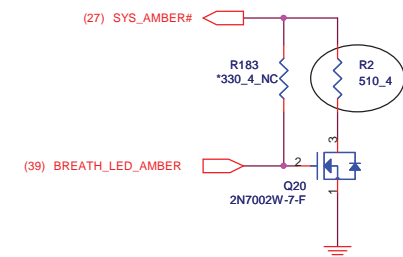
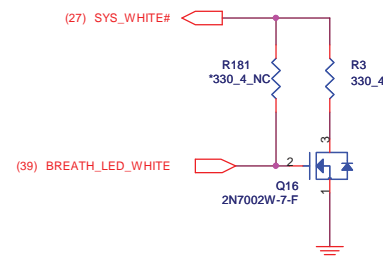
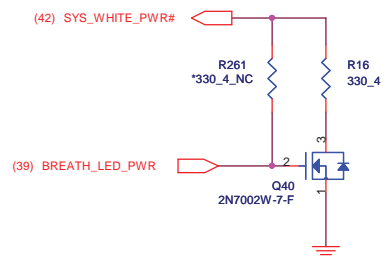
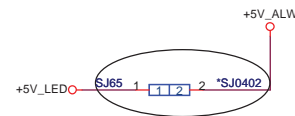
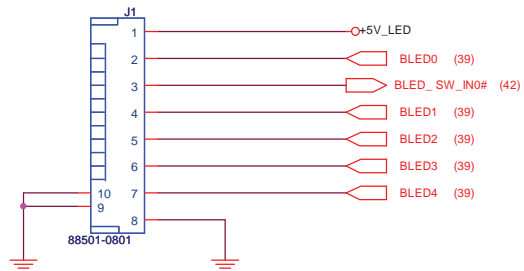


(20) VMC_DQ[63..0]
(20) VMC_DM[7..0]
(20) VMC_WDQS[7..0]
(20) VMC_RDQS[7..0]

CHANNEL B: 512MB/1024MB DDR3

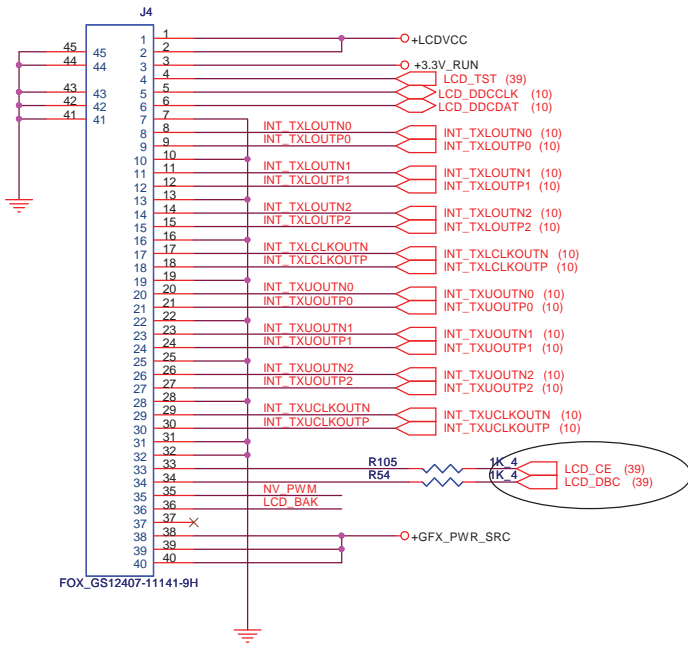


Conn to BLED Board



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PROJECT : SS8

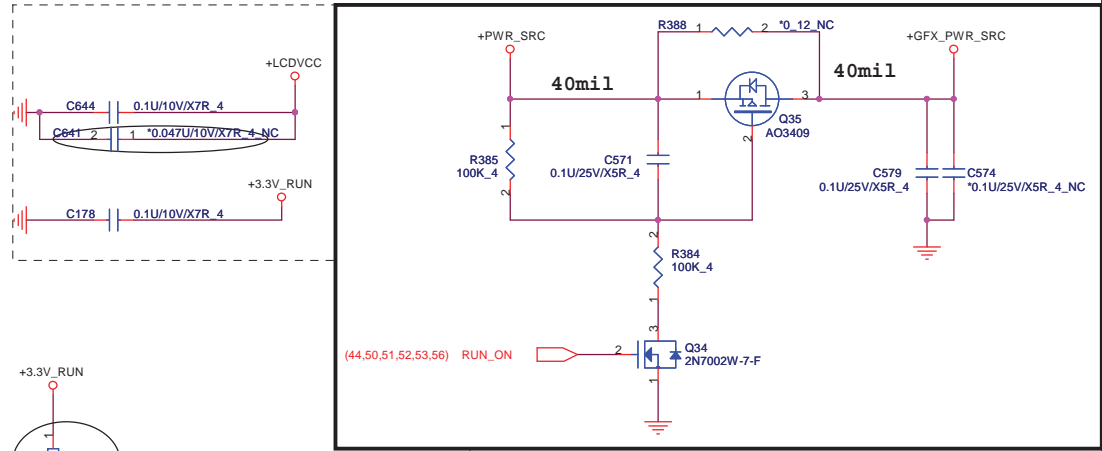
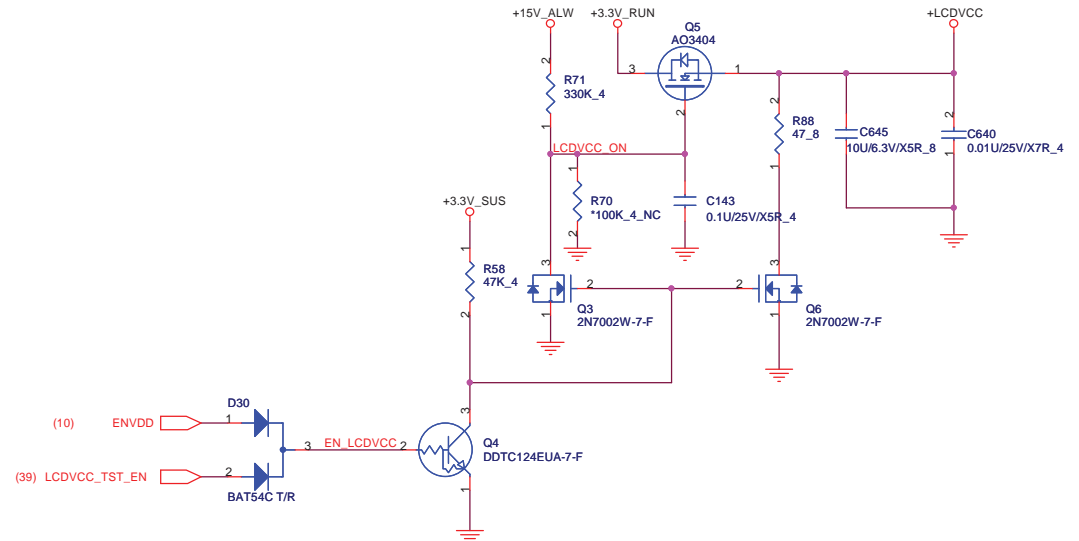
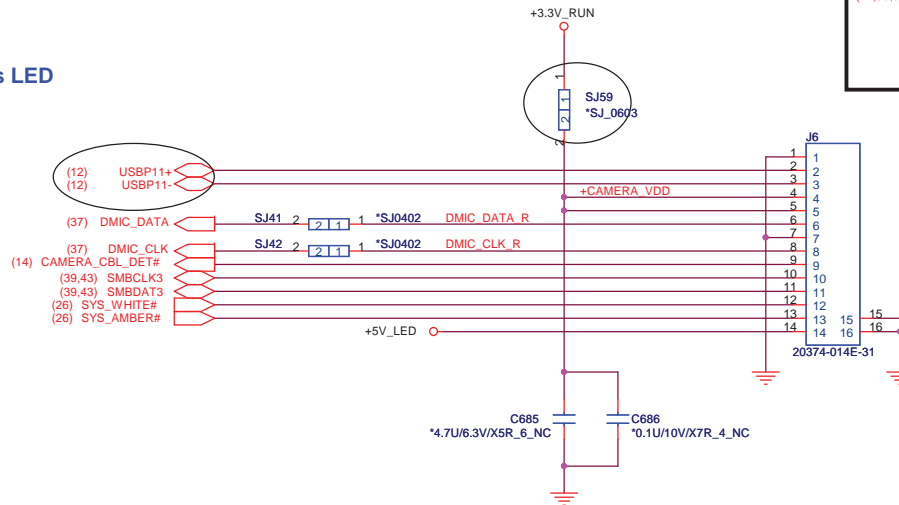
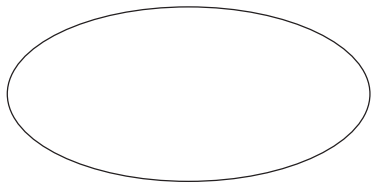
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EMC Reserve

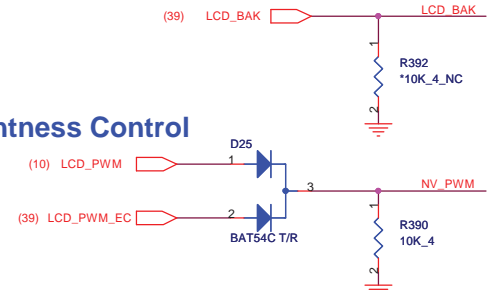
INT_TXLCLKOUTN	R411	1	2	*100_4 NC	INT_TXLCLKOUTP
INT_TXLOUTN2	R412	1	2	*100_4 NC	INT_TXLOUTP2
INT_TXLOUTN1	R416	1	2	*100_4 NC	INT_TXLOUTP1
INT_TXLOUTN0	R419	1	2	*100_4 NC	INT_TXLOUTP0
INT_TXUCLKOUTN	R400	1	2	*100_4 NC	INT_TXUCLKOUTP
INT_TXUOUTN2	R407	1	2	*100_4 NC	INT_TXUOUTP2
INT_TXUOUTN1	R408	1	2	*100_4 NC	INT_TXUOUTP1
INT_TXUOUTN0	R410	1	2	*100_4 NC	INT_TXUOUTP0

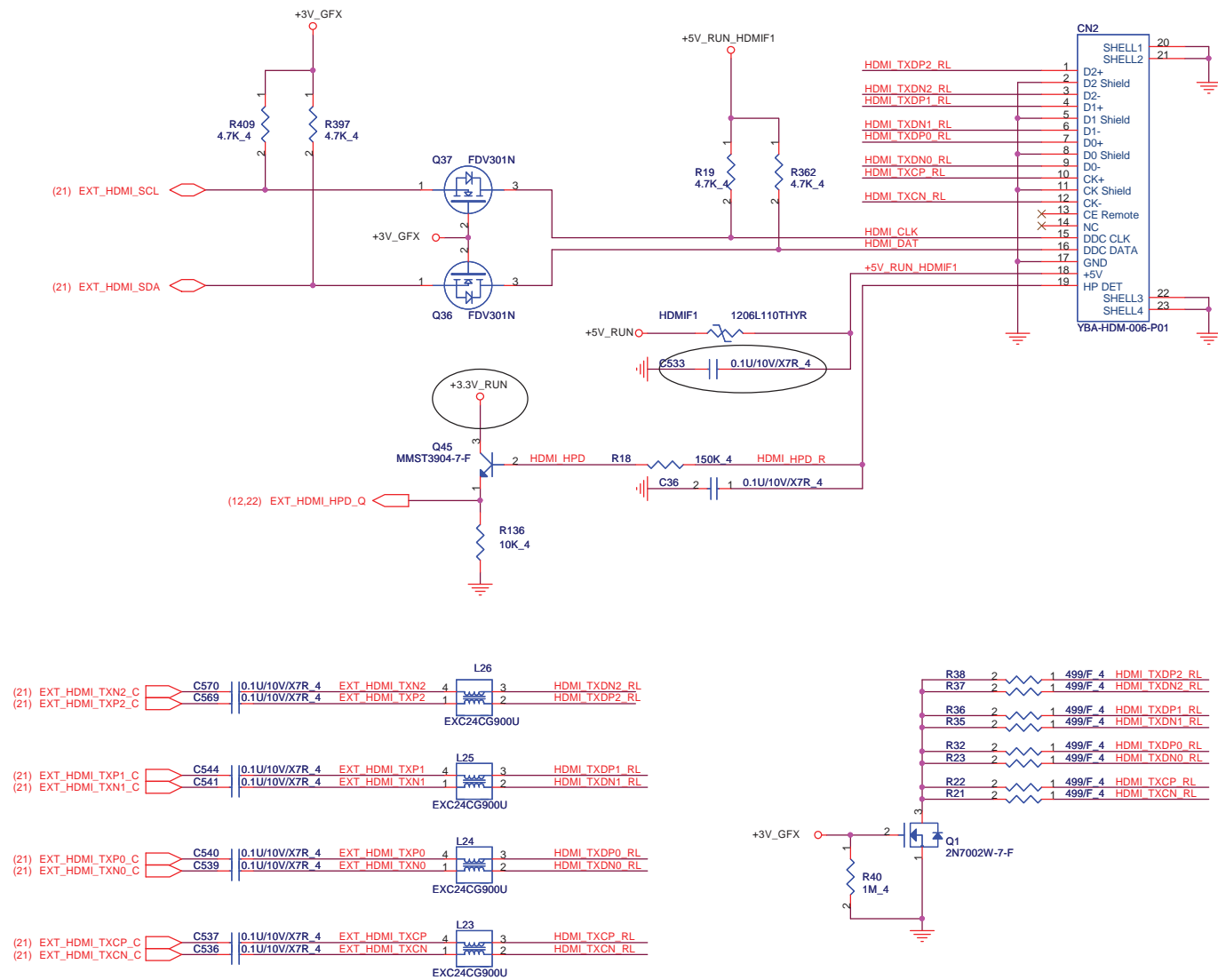
Array Microphone & Camera & System Status LED



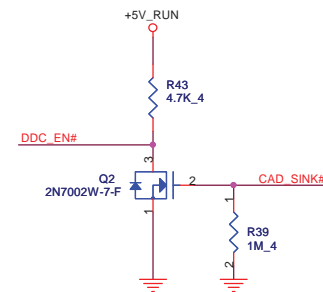
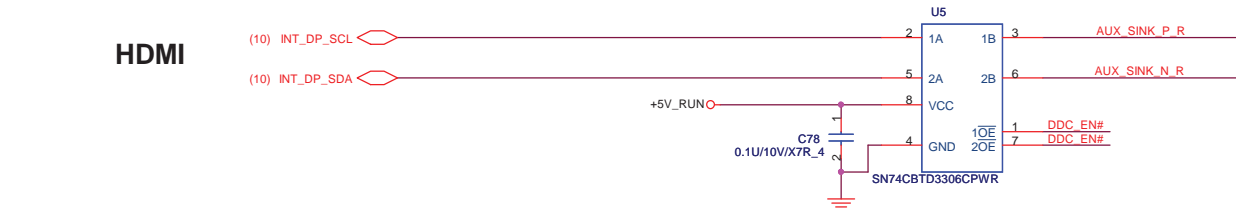
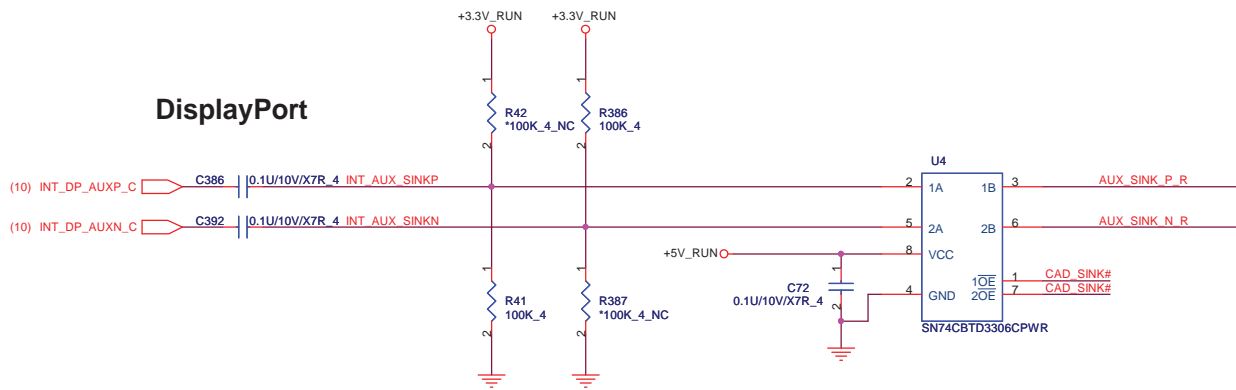
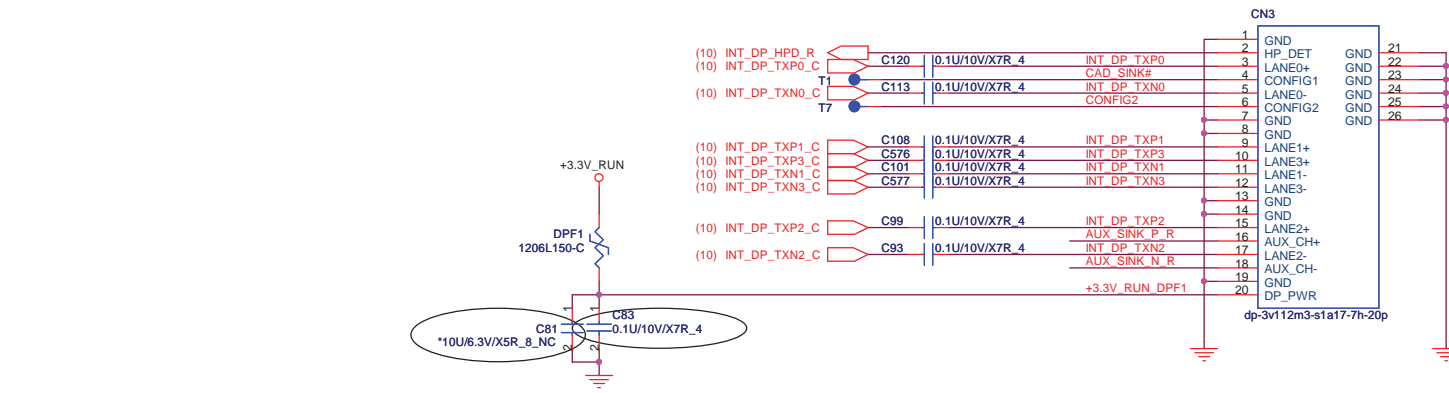
Backlight Enable

Brightness Control





MINI DISPLAY PORT CONNECTOR



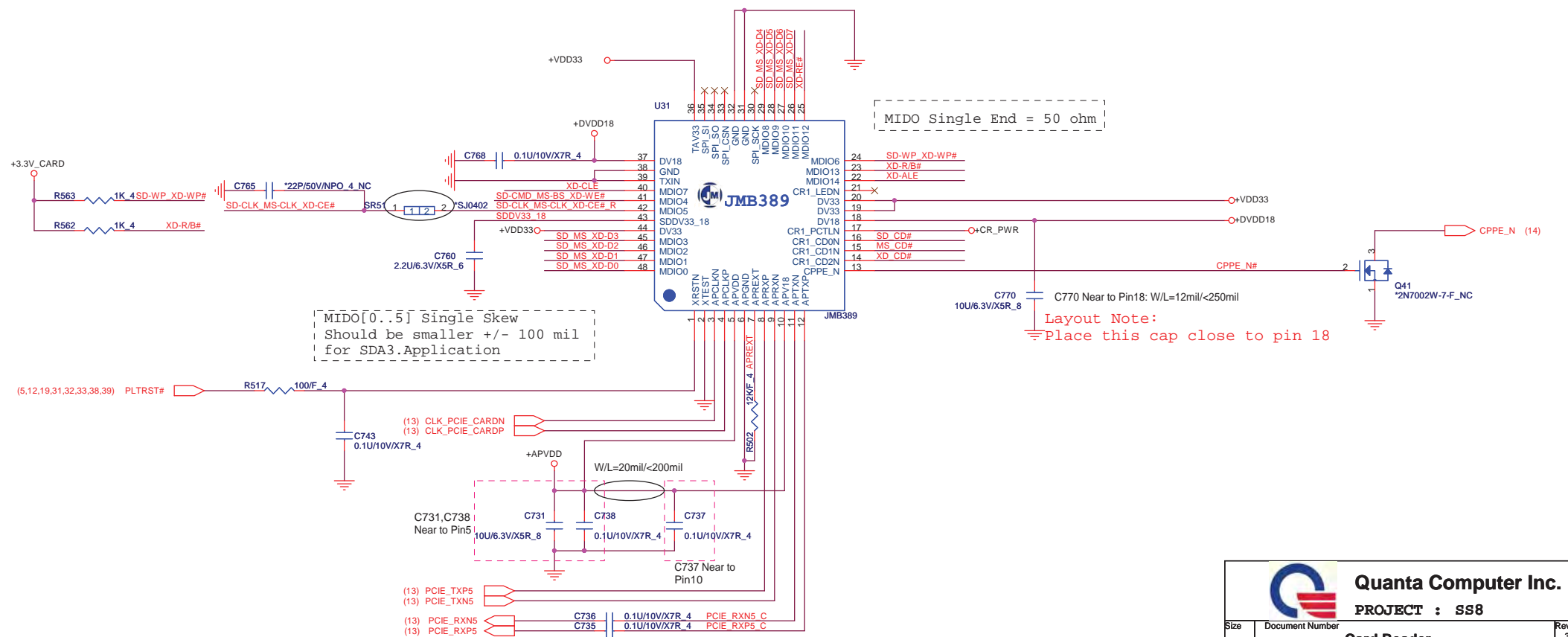
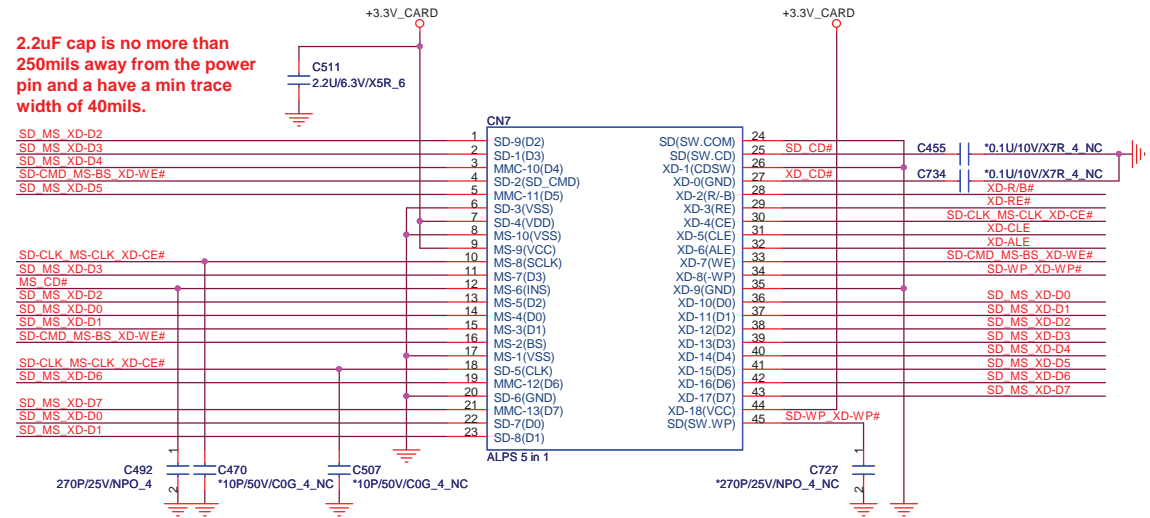
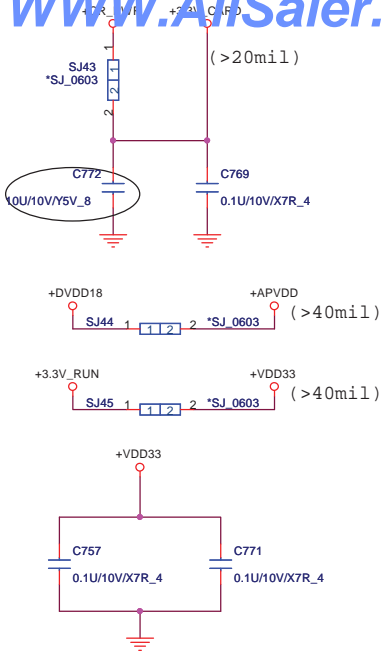
HDMI



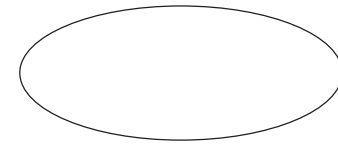
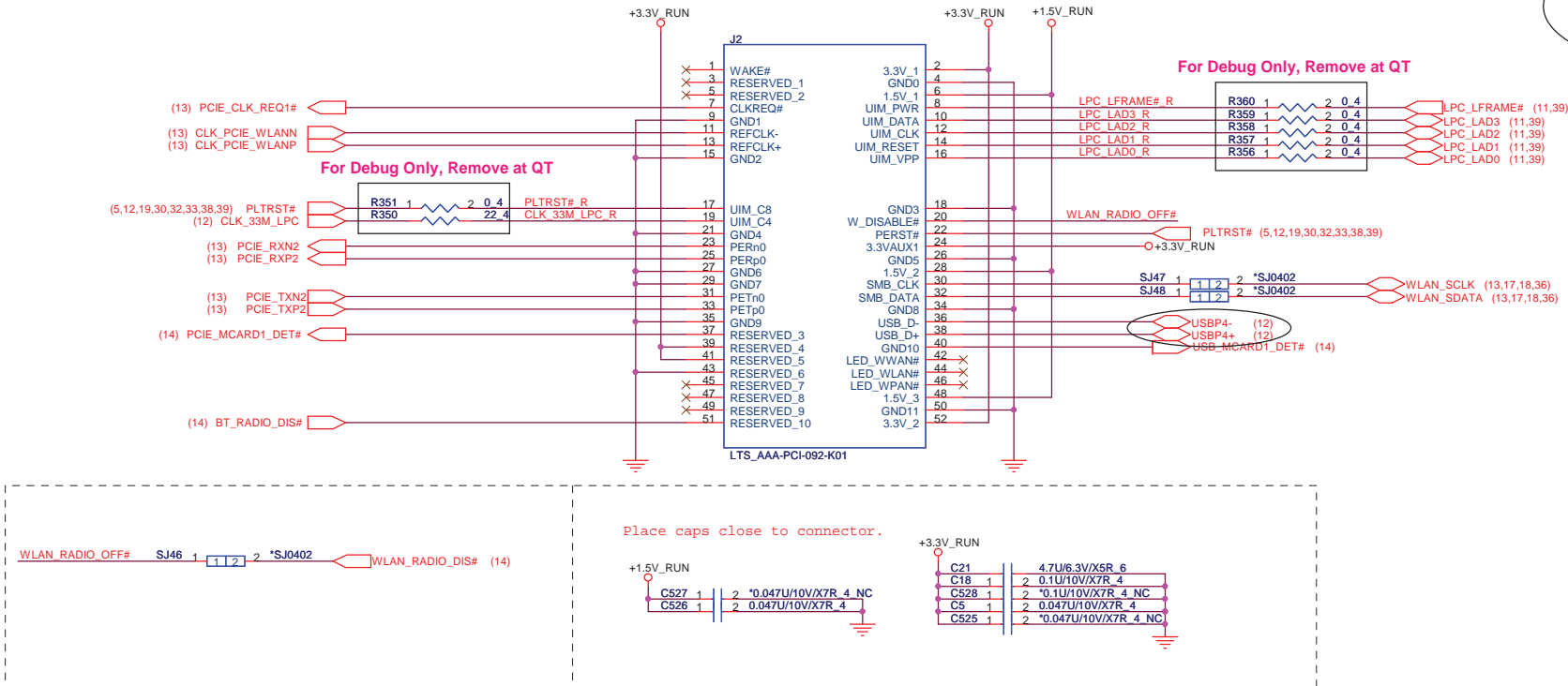
Quanta Computer Inc.
PROJECT : SS8

Card Reader interface signal mapping

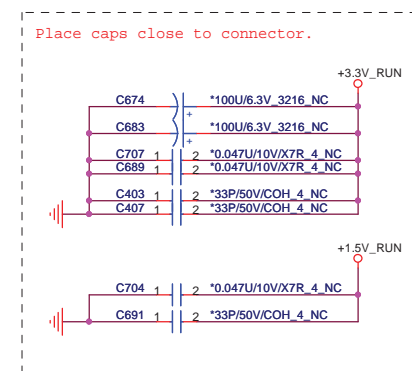
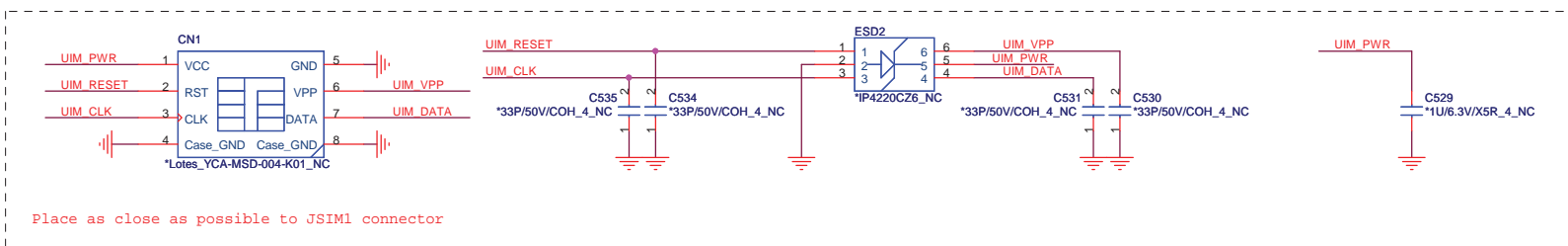
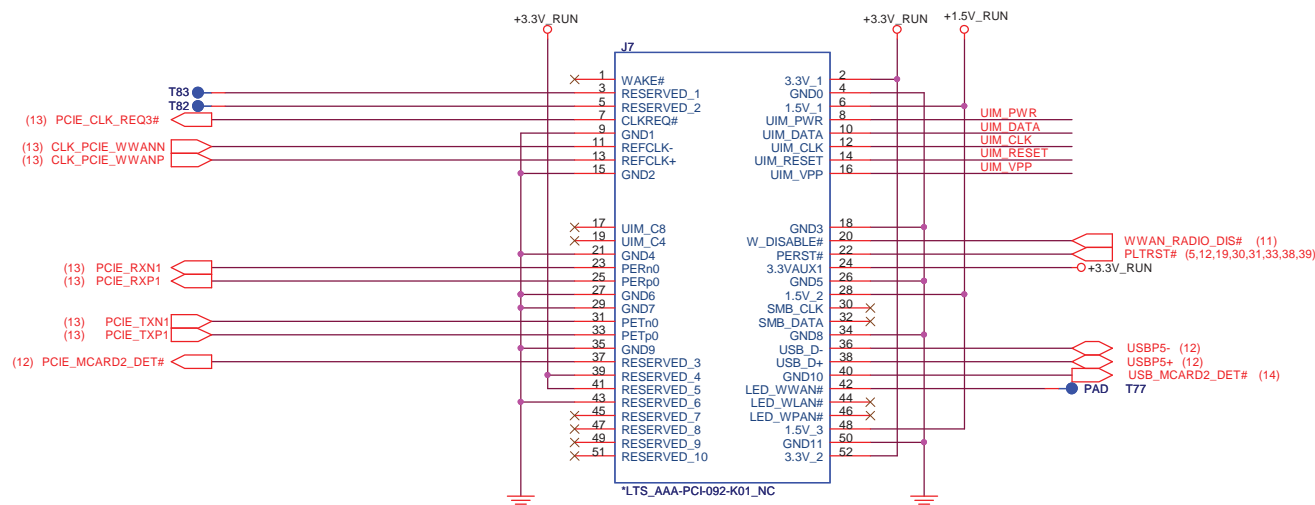
PIN	Default	SD / MMC	MS	XD
MDI000	SD/MMC/MS/xD	SD D0	MS D0	XD D0
MDI001		SD D1	MS D1	XD D1
MDI002		SD D2	MS D2	XD D2
MDI003		SD D3	MS D3	XD D3
MDI004		SD CMD	MS BS	XD WE
MDI005		SD CLK	MS CLK	XD CE#
MDI006		SD WP		XD WP#
MDI007				XD CLE
MDI008		MMC_D4	MS D4	XD D4
MDI009		MMC_D5	MS D5	XD D5
MDI010		MMC_D6	MS D6	XD D6
MDI011		MMC_D7	MS D7	XD D7
MDI012				XD RE#
MDI013				XD R/B#
MDI014				XD ALE
CR1_LED		SD_LED#	MS_LED#	XD_LED#
CR1_PCTL		SD_PWR#	MS_PWR#	XD_PWR#
CR1_CD0		SD_CD#		
CR1_CD1			MS_CD#	
CR1_CD2				XD_CD#

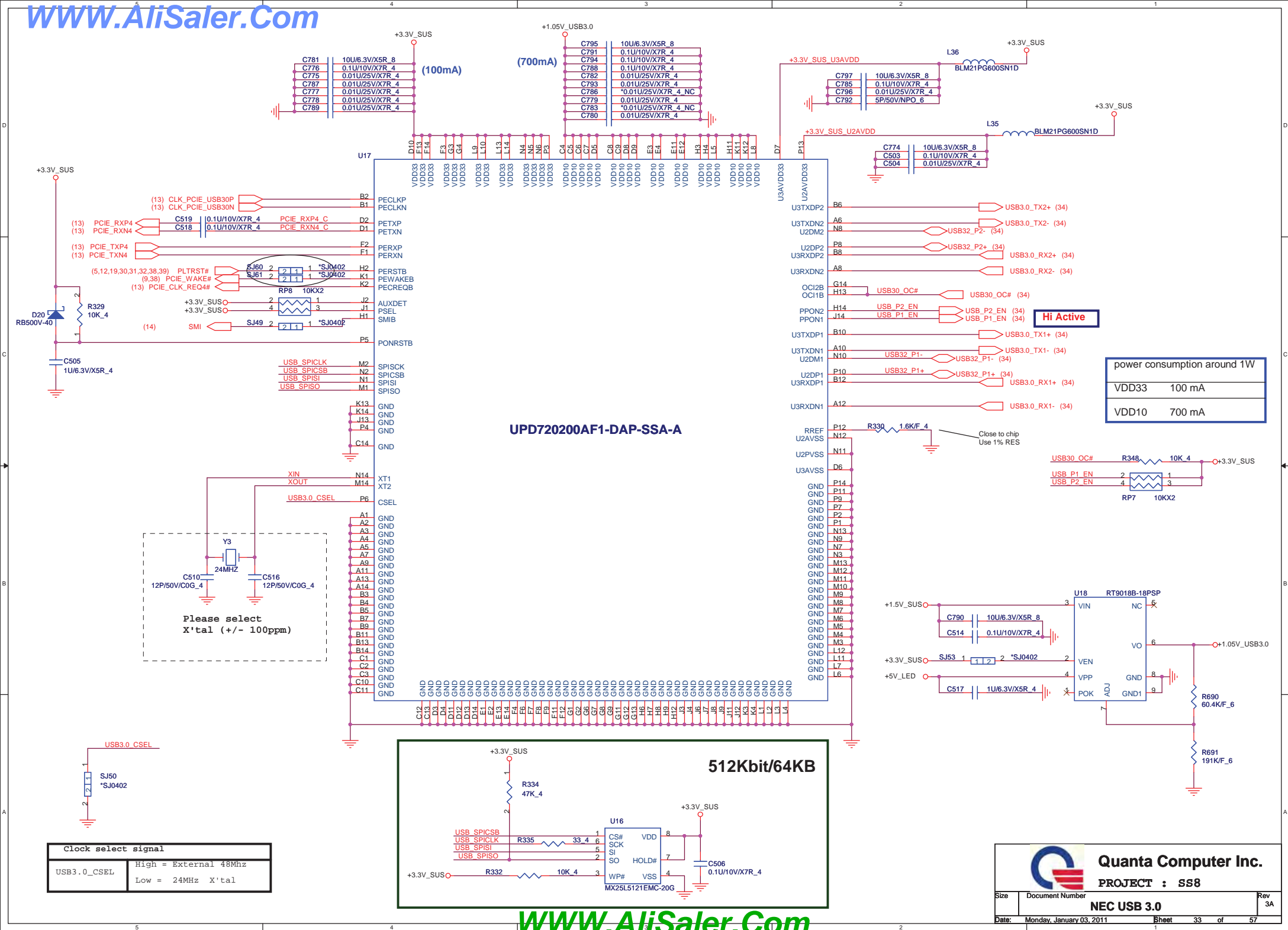


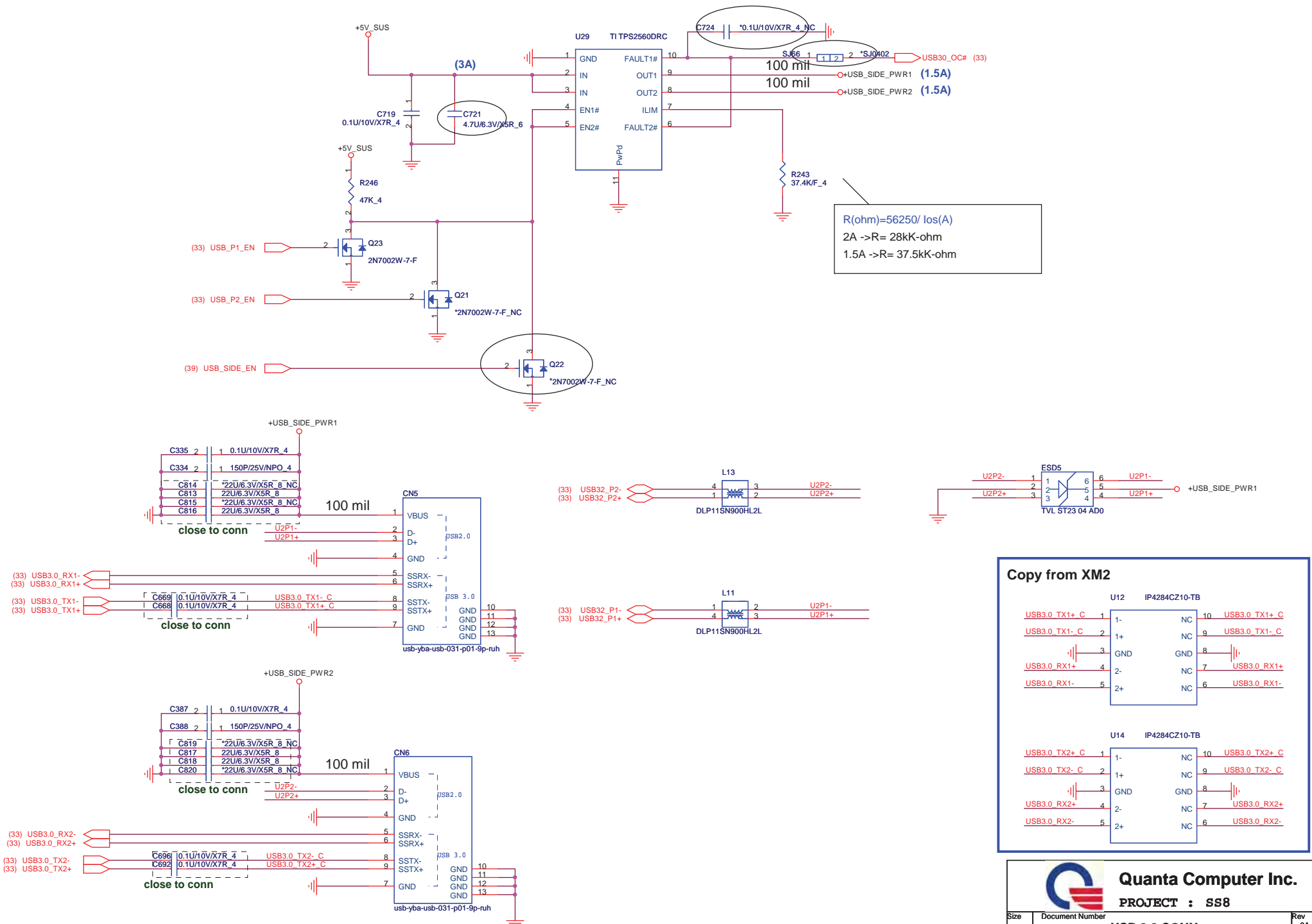
MiniCard WLAN connector



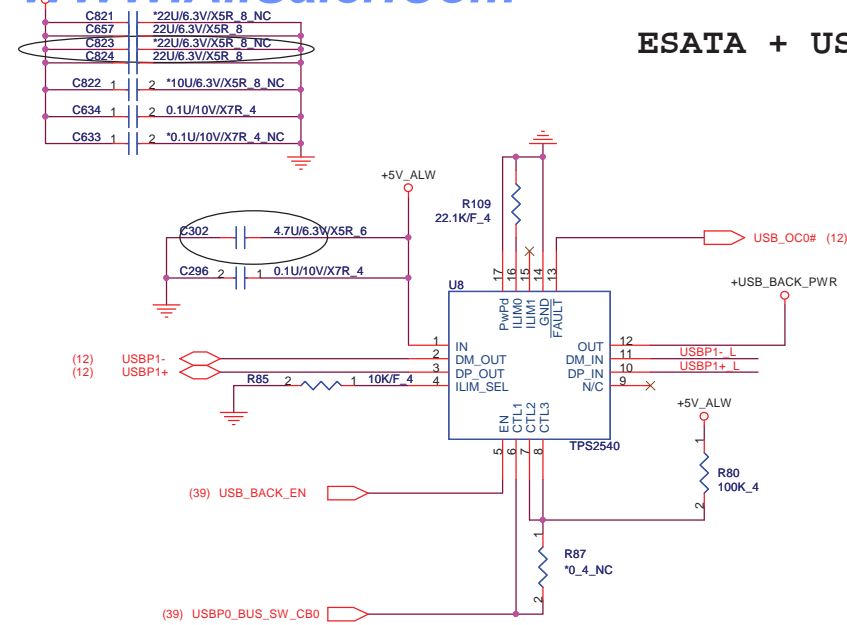
MiniCard WWAN connector







ESATA + USB Conn + Power share



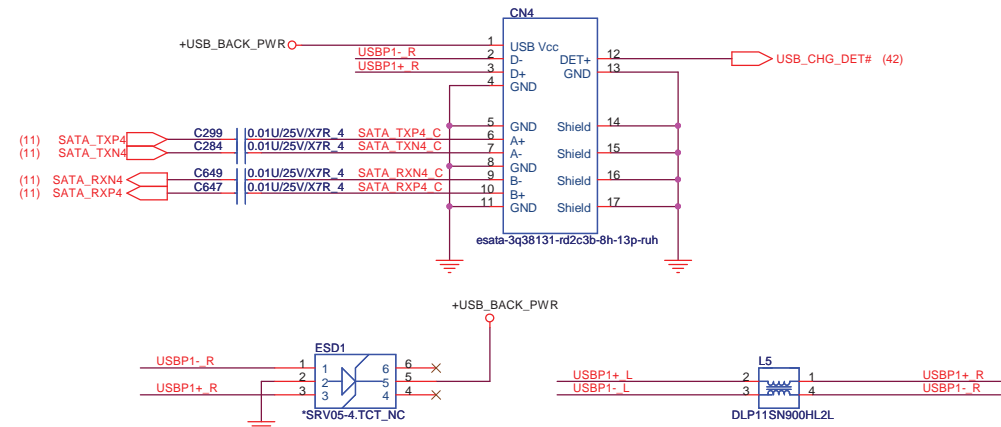
ES(PG1.0): Stuff R87, Un-Stuff R80
MP(PG1.1): Un-Stuff R87, Stuff R80

USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

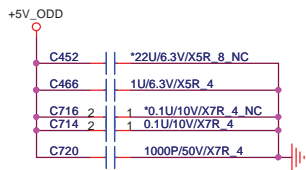
	R109	mA
OC limitation	100k ohm	480
	22.1k ohm	2171

Applied Now

E-SATA Conn

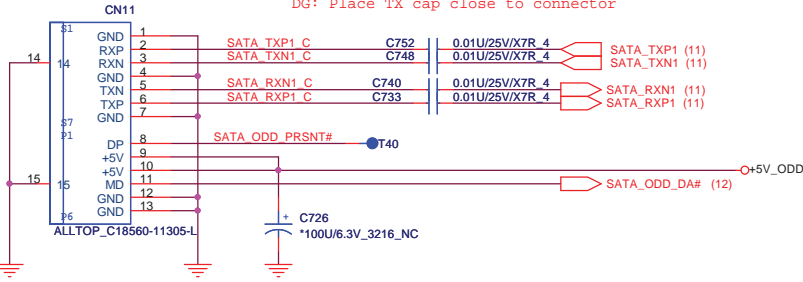


Place caps close to CN11.

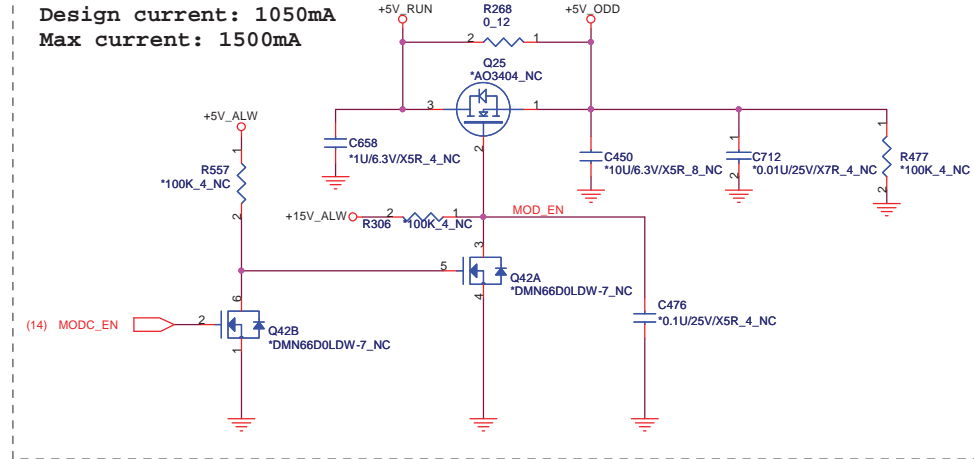


ODD Connector

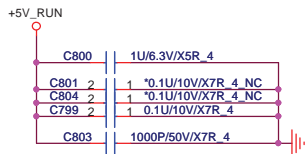
DG: Place TX cap close to connector



Design current: 1050mA
Max current: 1500mA

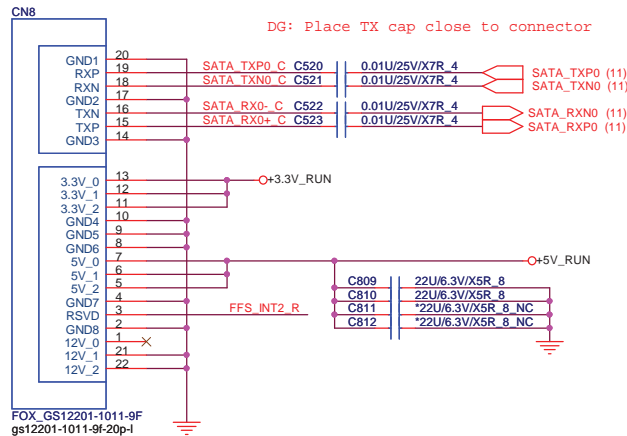


Place caps close to CN8.

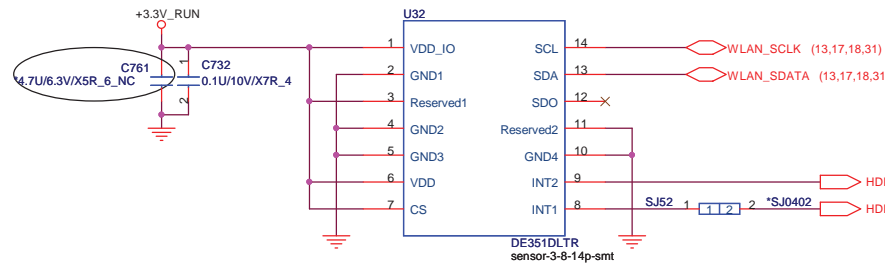


SATA Connector.

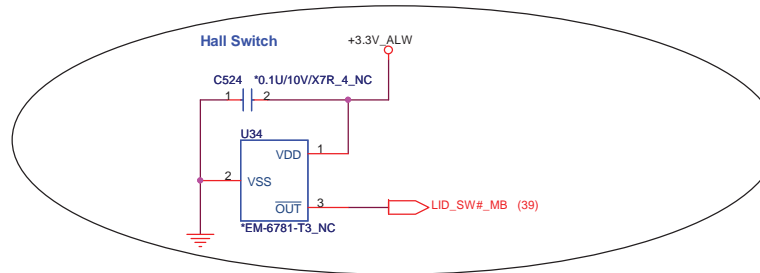
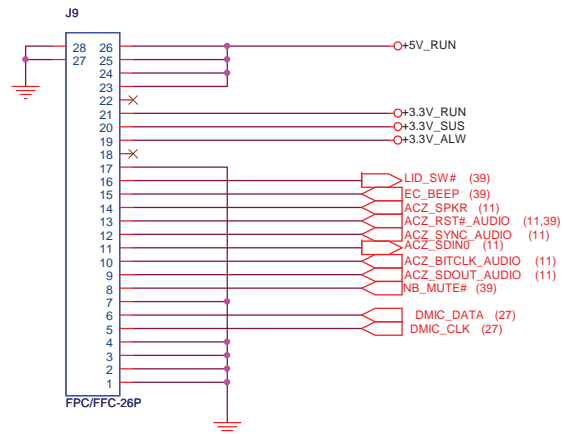
DG: Place TX cap close to connector

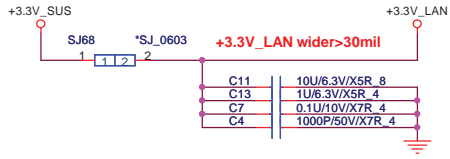


3-axis Fall Sensor (HDD data protector)



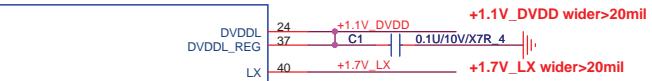
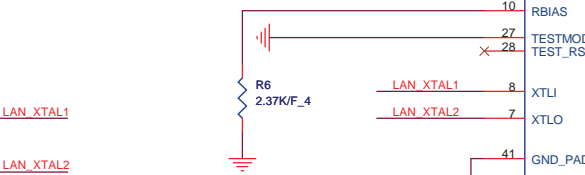
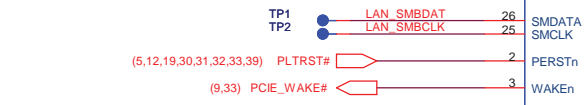
CONNECT TO AUDIO BOARD



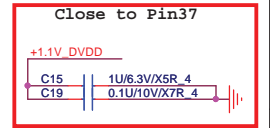
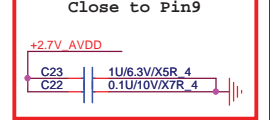
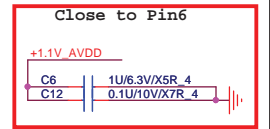
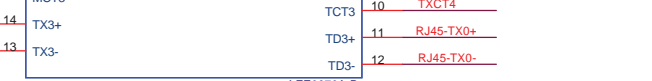
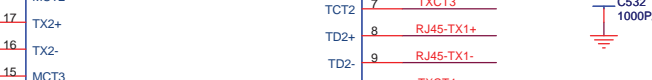
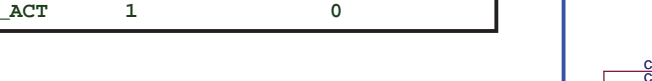
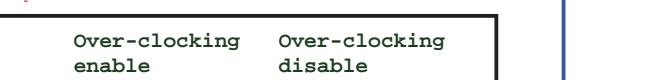
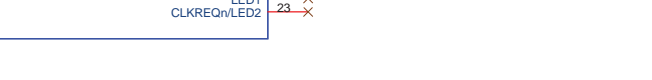
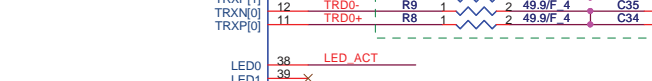
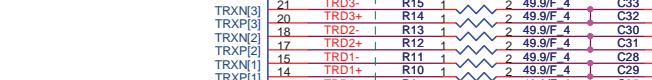
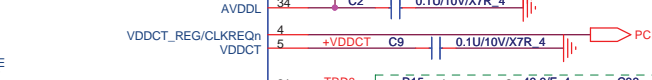
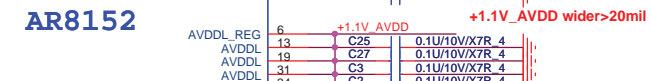
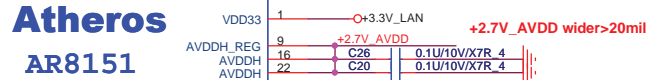


Atheros
AR8151
AR8152

AR8151B

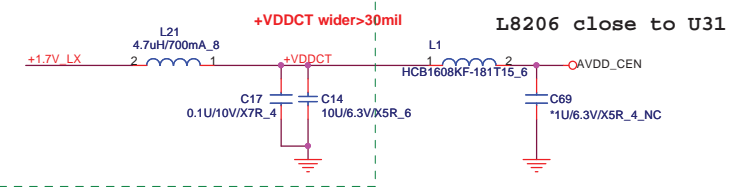


Netlist delete
Pin13 &19

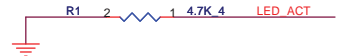


Close to LAN chip

Close to pin40



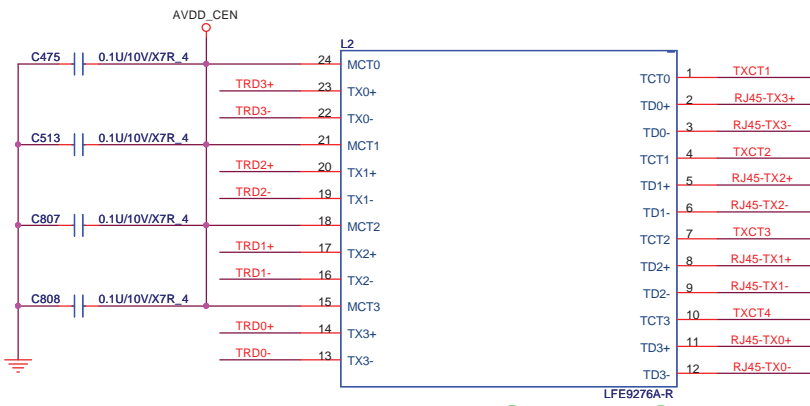
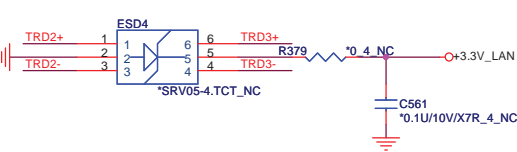
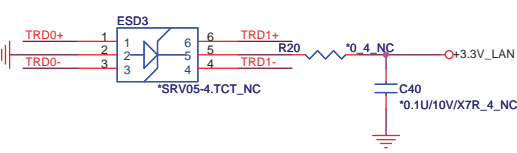
L8206 close to U31



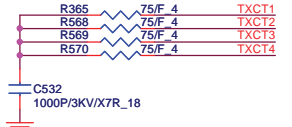
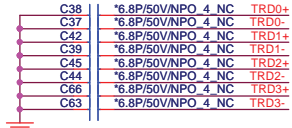
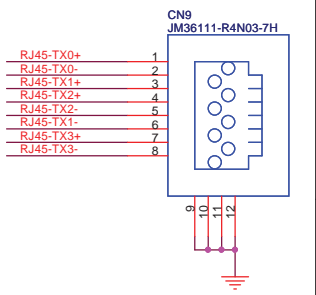
Over-clocking
enable
LED_ACT 1

Over-clocking
disable
LED_ACT 0

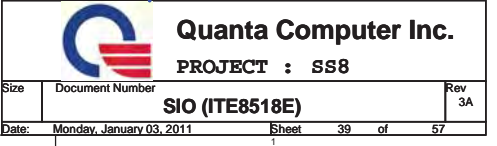
Change to CM1293A-04SO



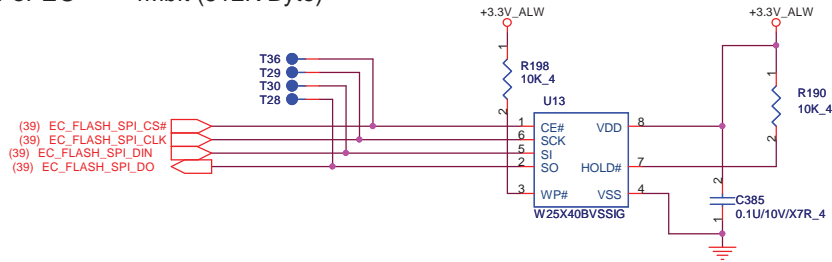
RJ-45 Connector



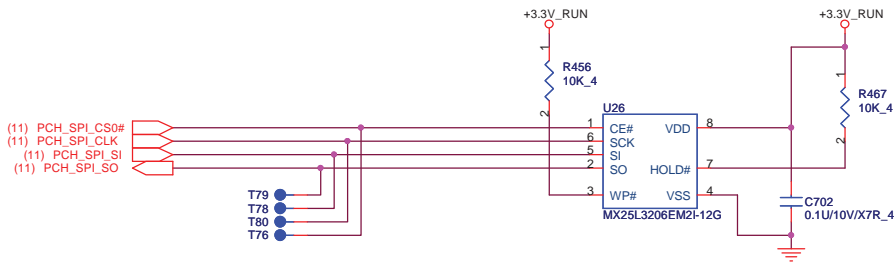
Wait for Connector list to update



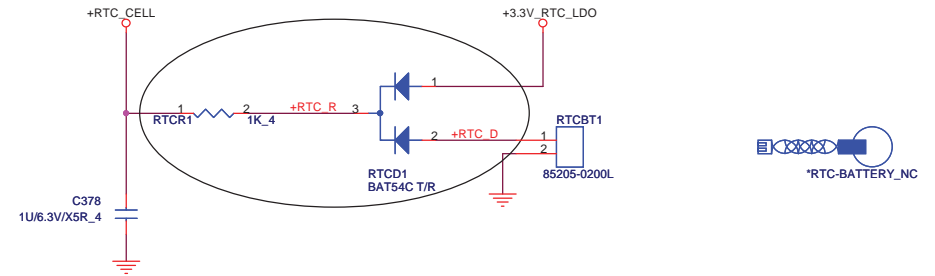
For EC 4Mbit (512K Byte)



For PCH 32Mbit (4M Byte)



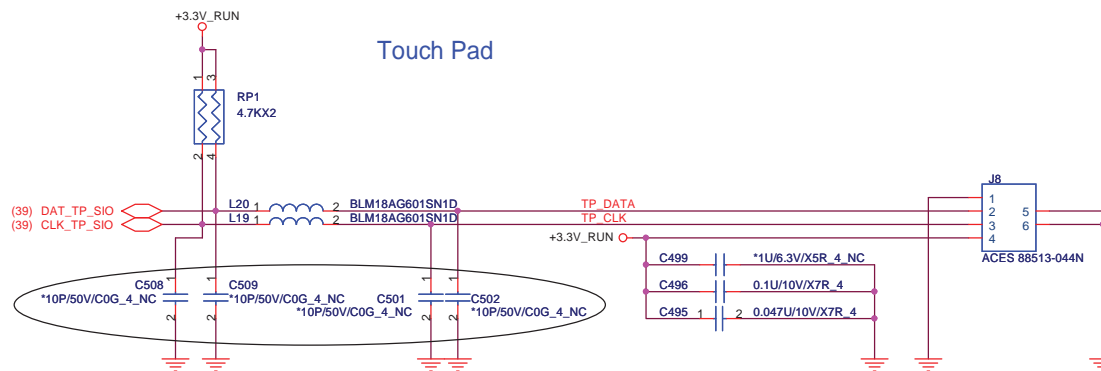
RTC BATTERY



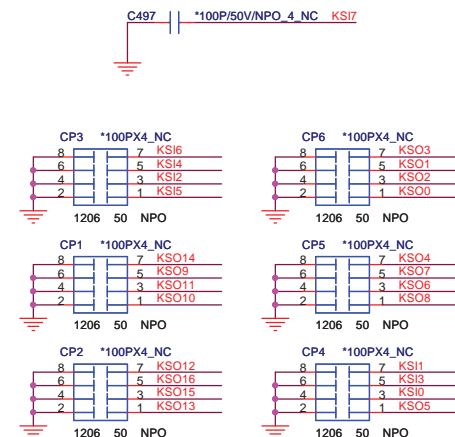
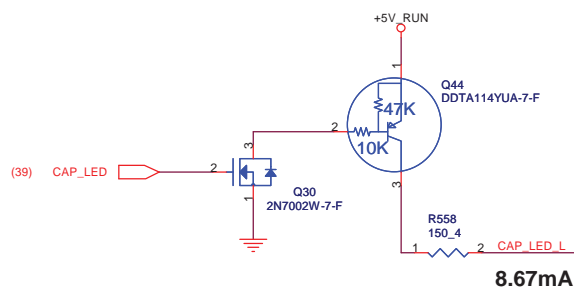
Quanta Computer Inc.

PROJECT : SS8

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	FLASH / RTC	3A
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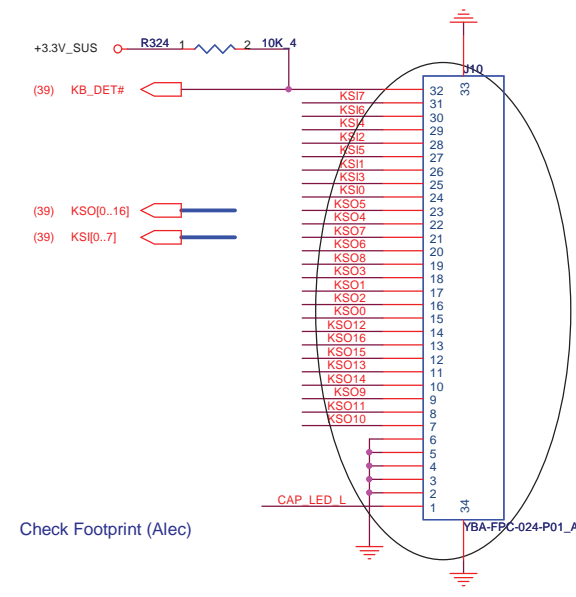


$V_{i(on_max)} = -1.4V$
 $V_{i(off_min)} = -0.3$



100P CAPS CLOSE TO JKB1

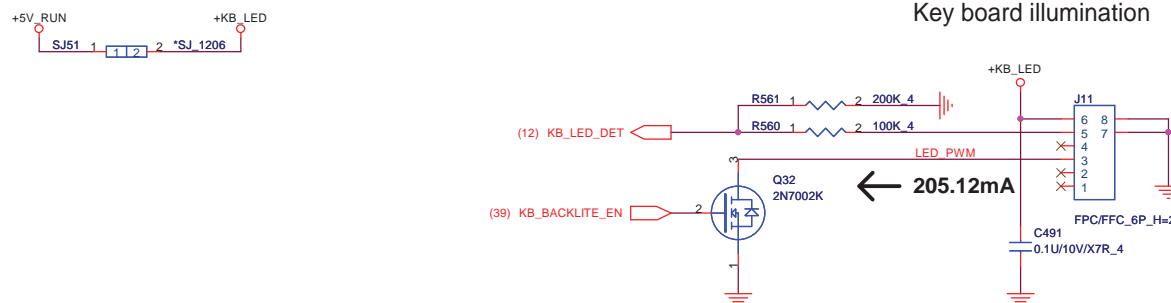
KEYBOARD CONNECTOR



Conn Copy From SS7

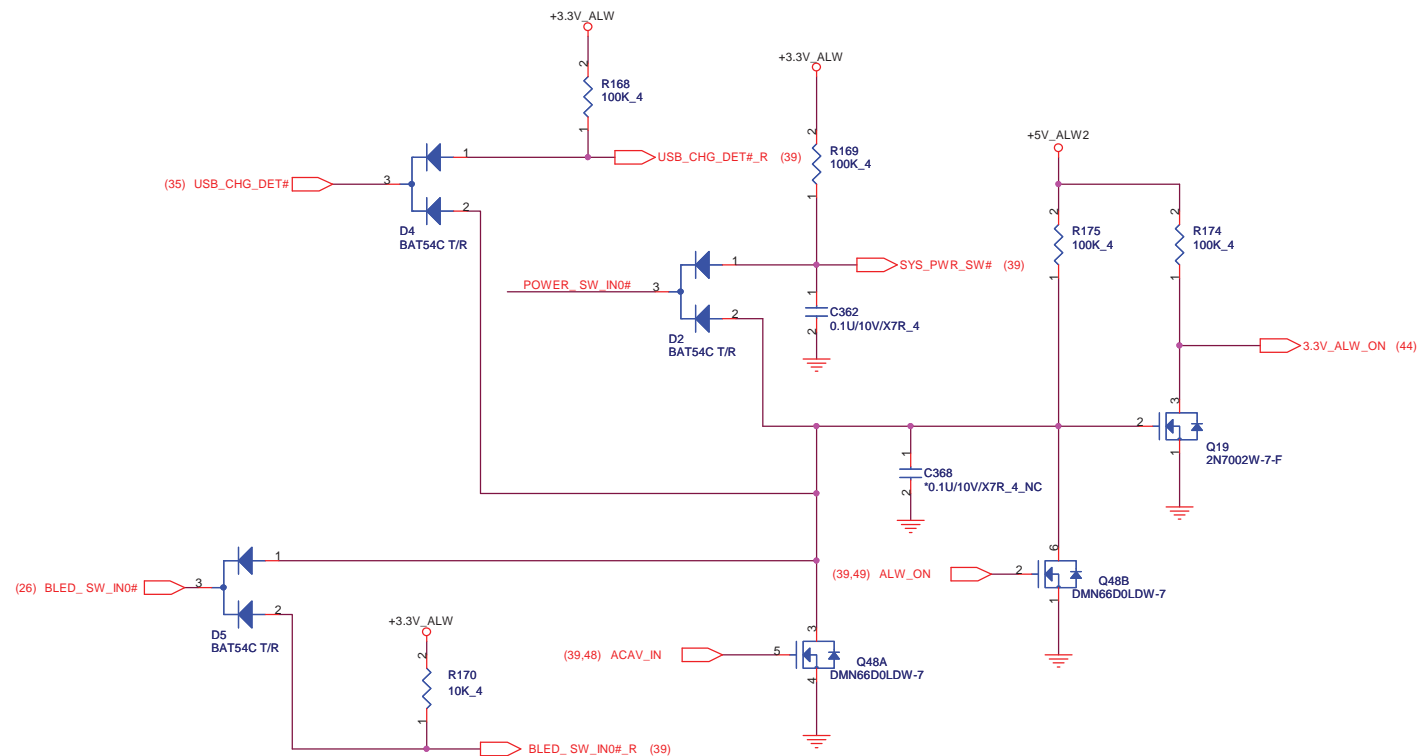
+KB_LED power trace width >10 mil

Key board illumination

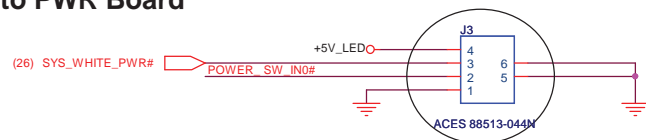


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 PROJECT : SS8

3VALW ON POWER LOGIC



Conn to PWR Board



Status White LED

Solid White= System On, Normal Activity
 Solid White= Charging (system on);
 Solid White= Charging (system off or hibernate and battery charge <98%);
 OFF= Charging (system off or hibernate and battery charge > 98%);
 "Breathing White " = System in Standby (S3);
 Off = System Off (or in Hibernate);



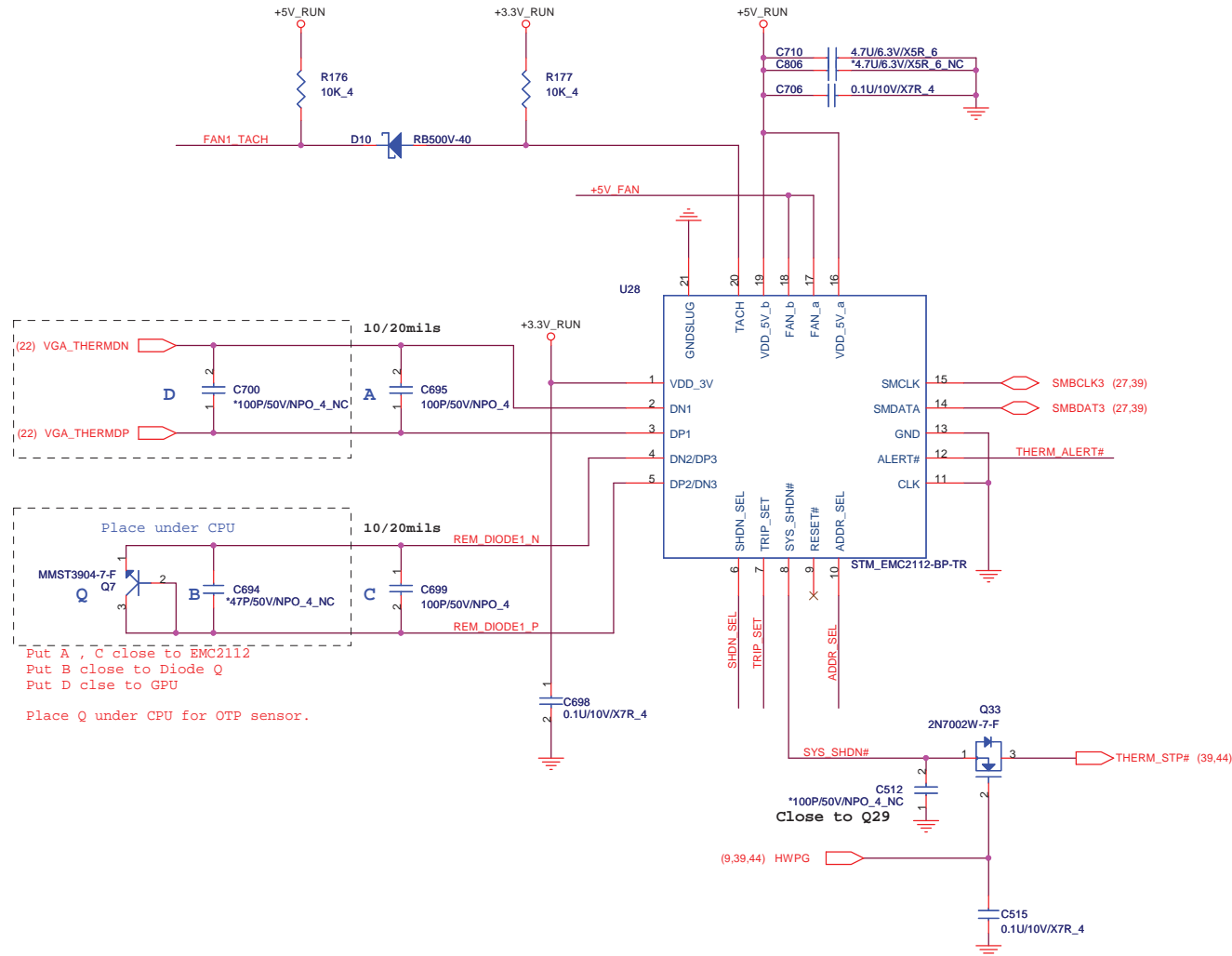
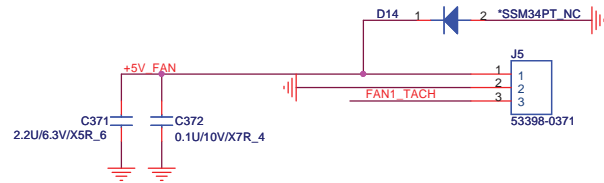
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PWR SW/LED

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FAN CONTROL



Put A, C close to EMC2112
Put B close to Diode Q
Put D close to GPU
Place Q under CPU for OTP sensor.



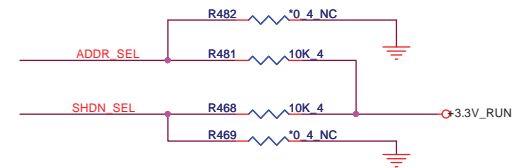
EMC2112 internal diode should be set 90 degree C (EC)

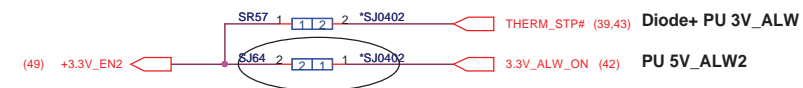
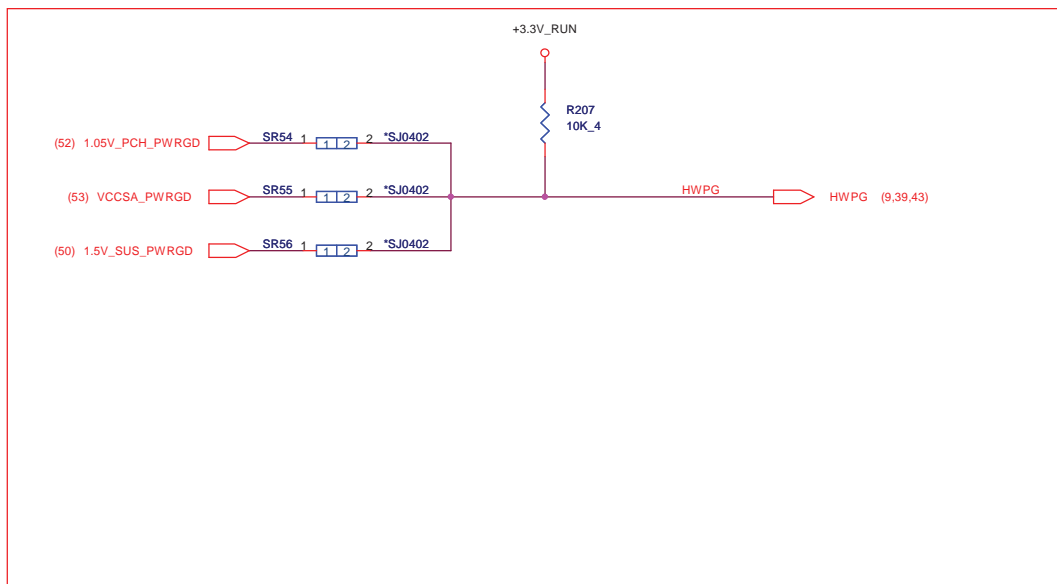


OTP Trip Point: 90 °C
OTP Hysteresis: 85 °C (Vincent)

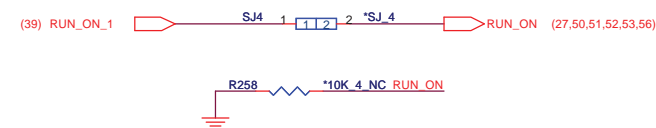
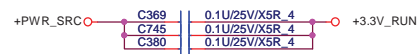
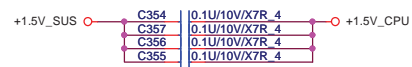
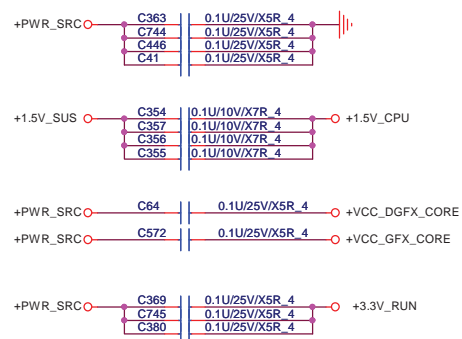
Need to check with BIOS
ADDR_SEL
HIGH: 0101 110xb
OPN: 0111 101xb
GND: 0101 111xb

SHDN_SEL
HIGH: External Diode 2 Mode
OPN: AMD CPU/Diode Mode
GND: Intel Transistor Mode





Stitch Cap



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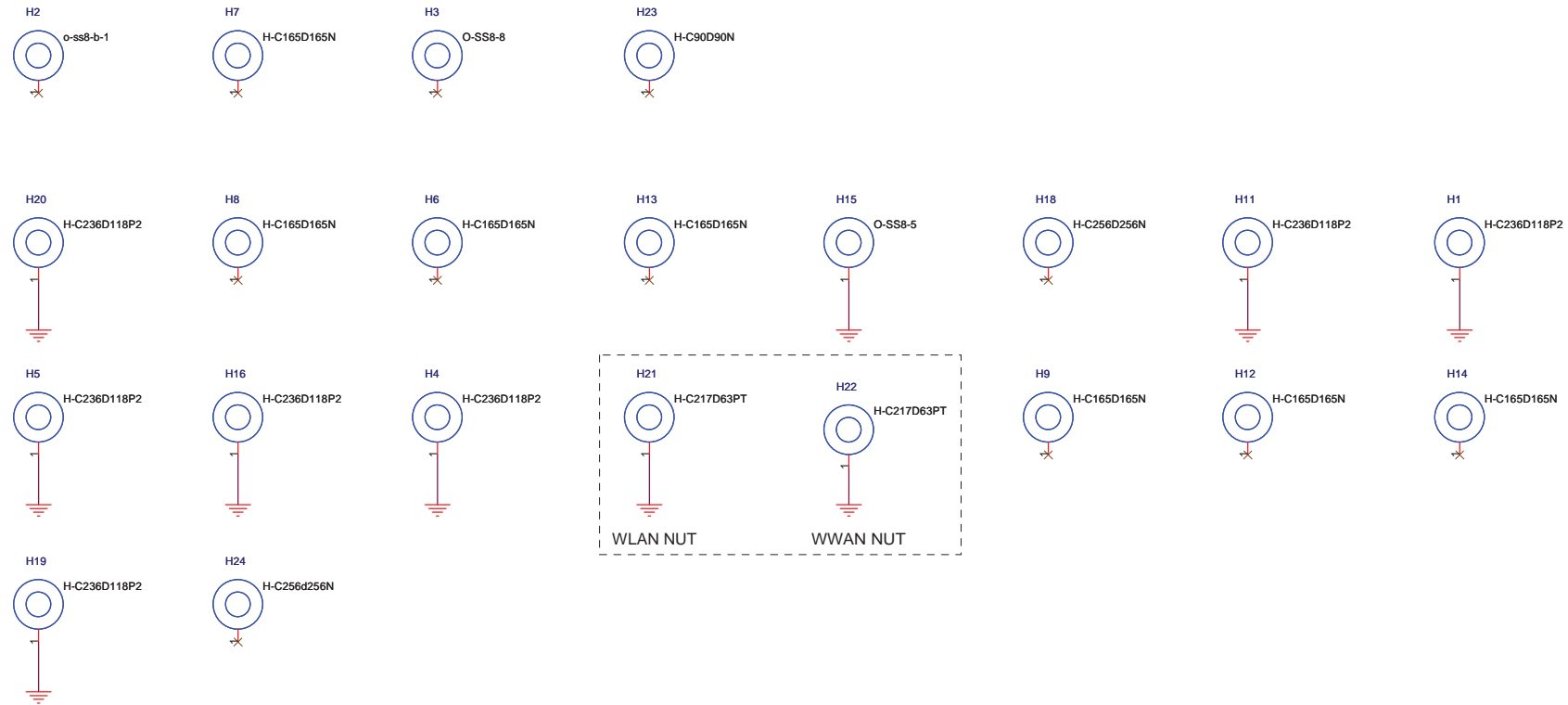
Size	Document Number	Rev
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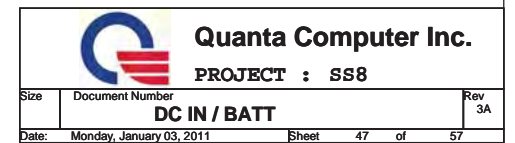
System Reset Circuit

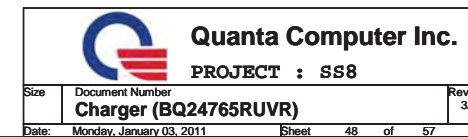
CPU XDP

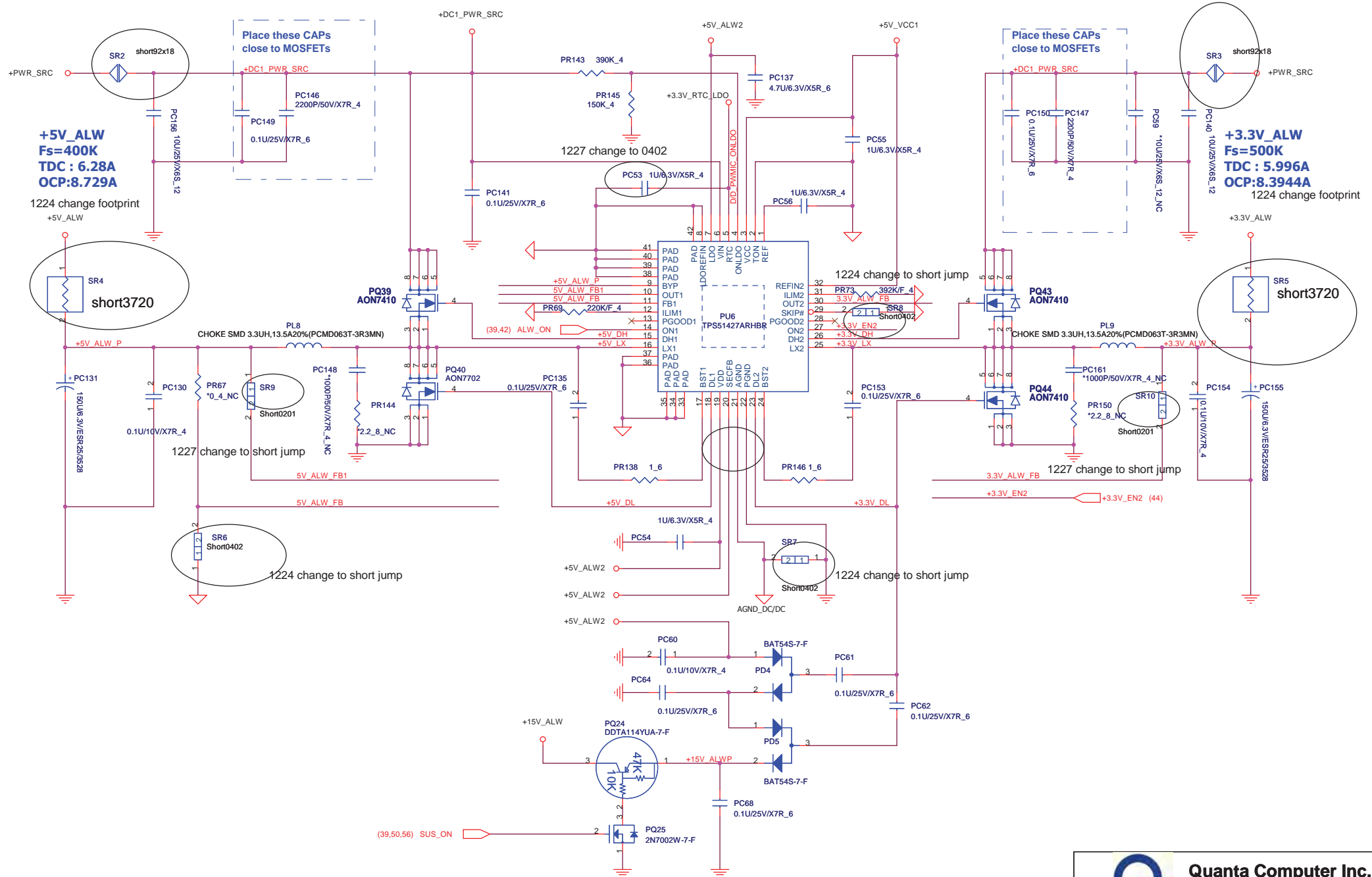
PCH XDP

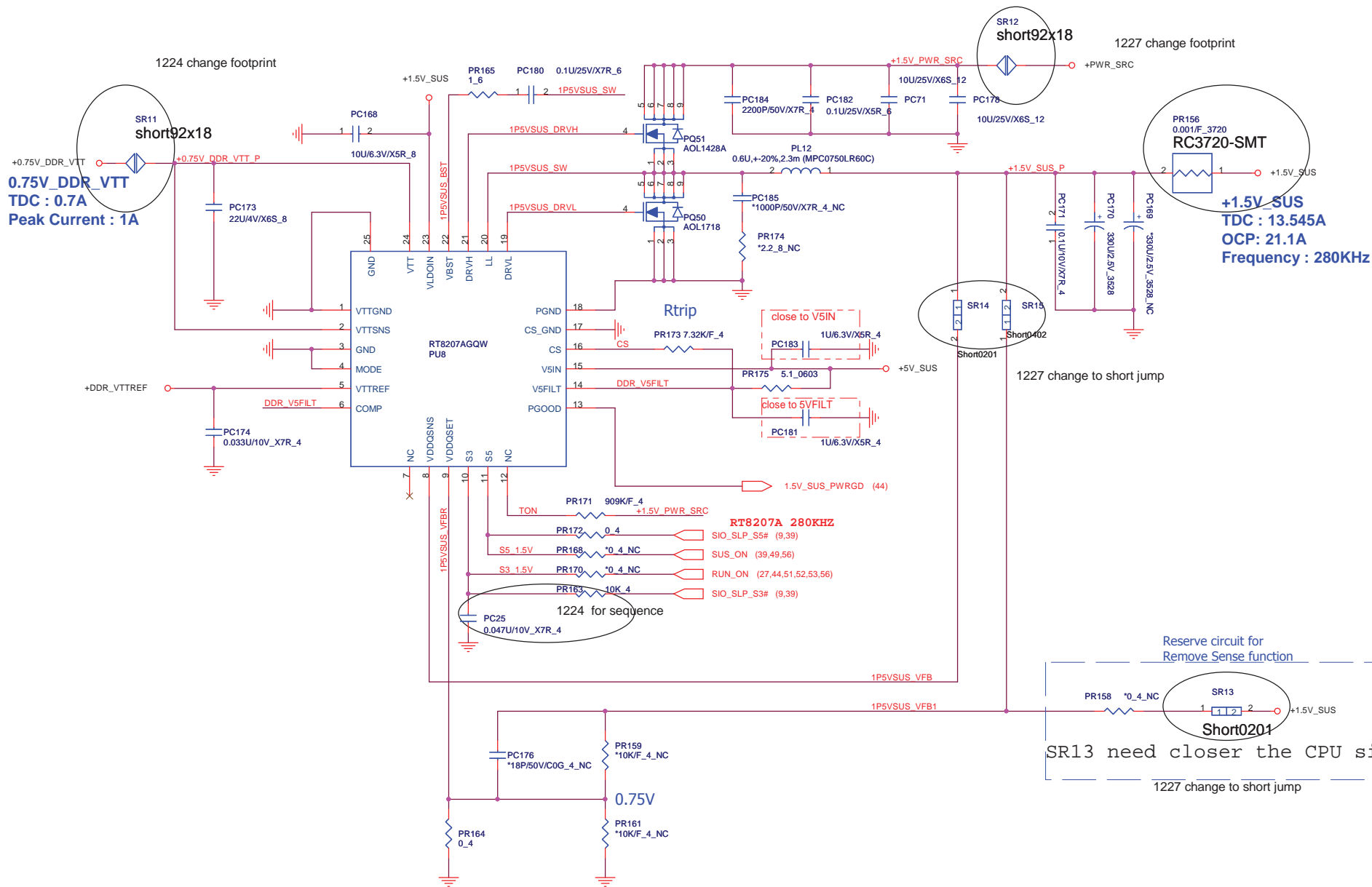
Del 0420







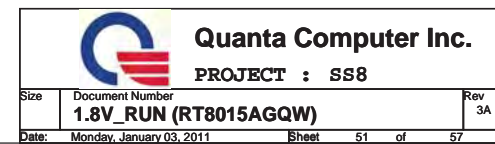




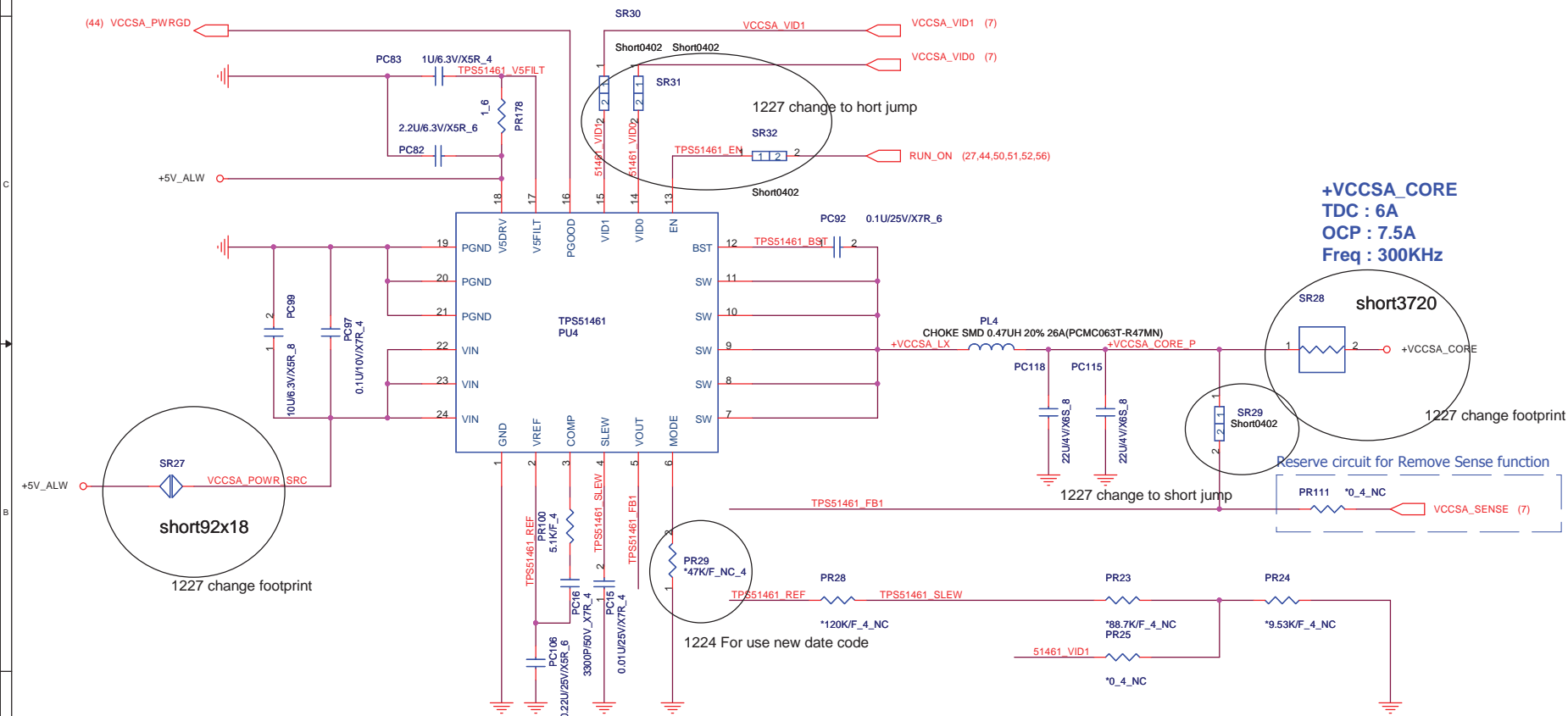
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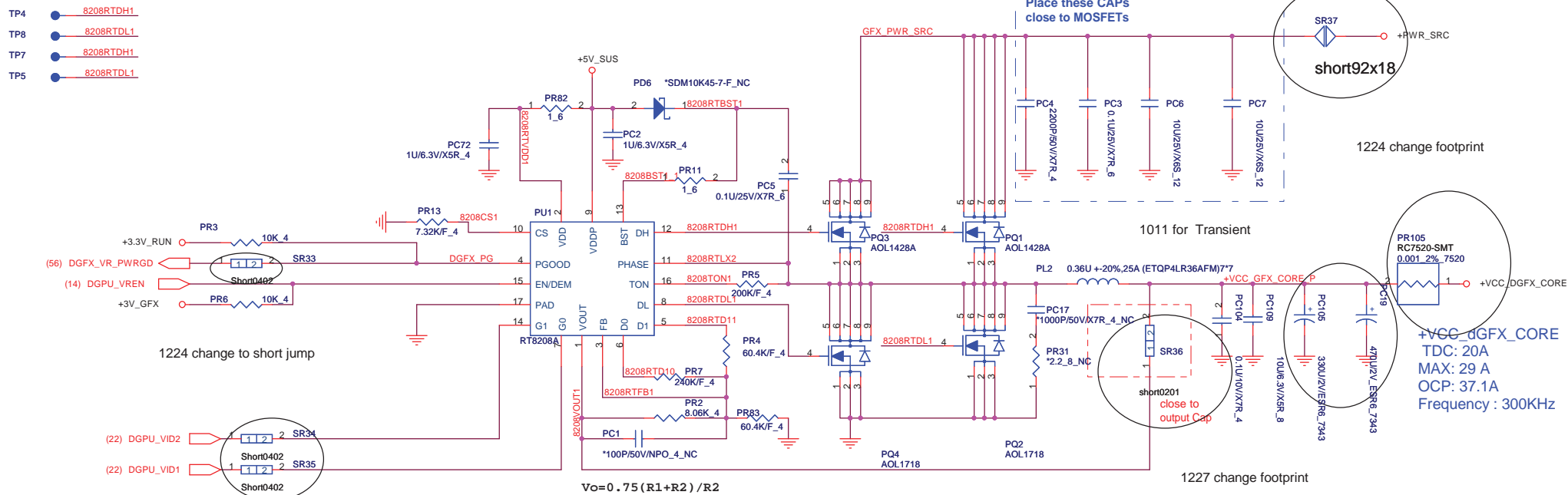
Size	Document Number	Rev
1	1.5_SUS/0.75_DDR_VTT (RT8207AGQW)	3A
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+VCCSA	VCCSA_VID1	
0.8V	High	
0.9V	Low	Apply now

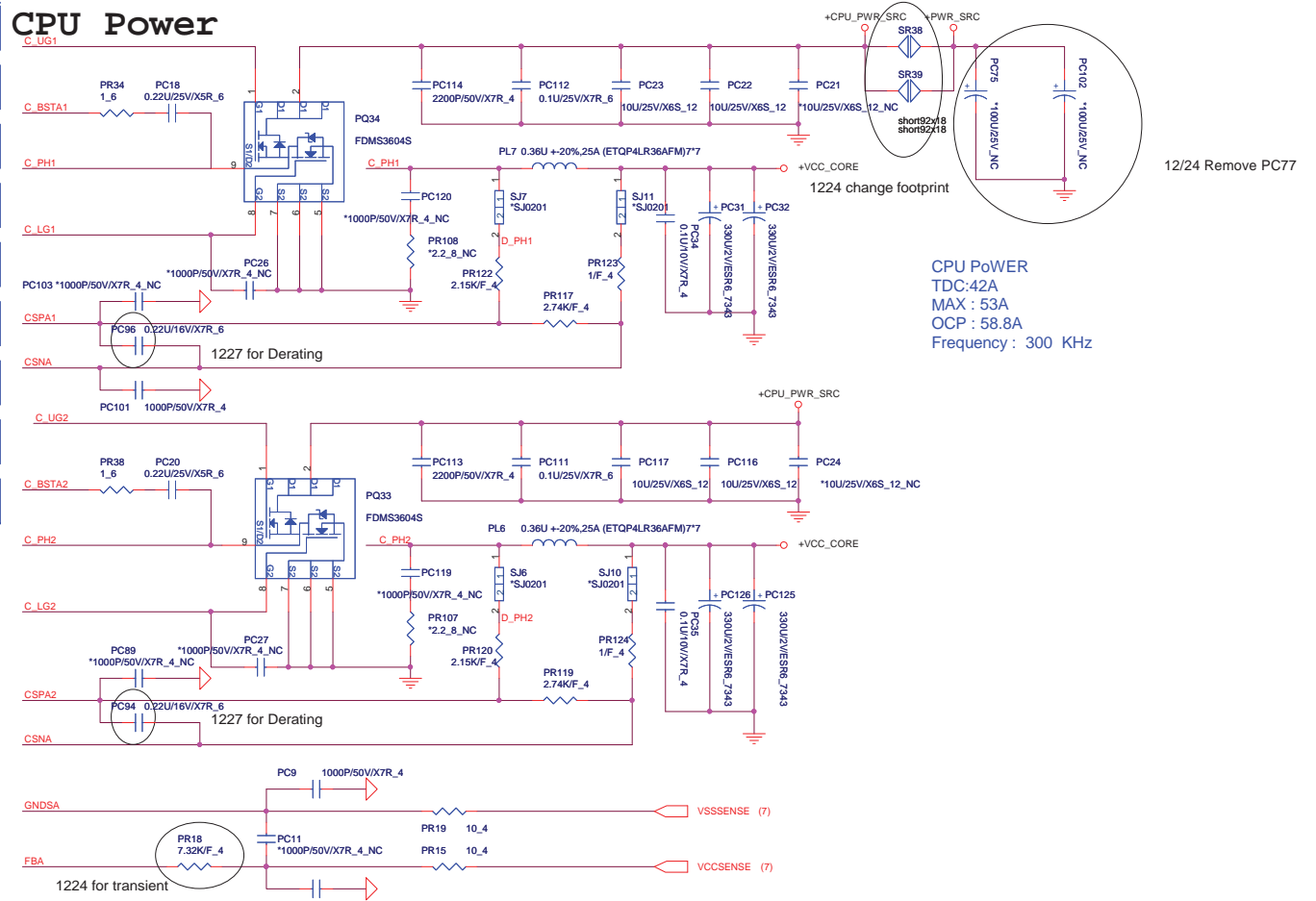
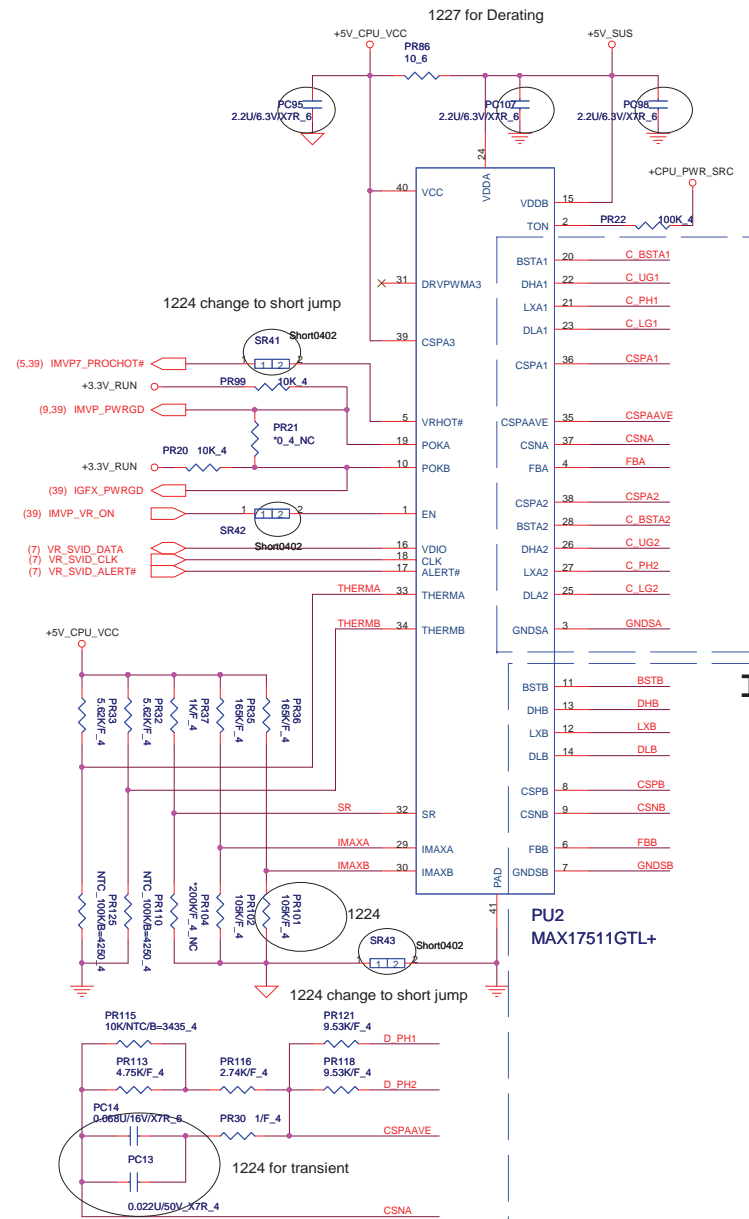


```
+VCC_GFX_CORE
Control IC: RT8208A
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7670(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.36uH +-20% 45A(MP0104F-R36H1)(Delta), DCR=0.89mohm
Output Cap: 2*390uF, 2.5V(20%,105C,6.3*5.8), ESR=10mohm
```

DGPU_VID1	DGPU_VID2	+VCC_GFX_CORE
LOW	LOW	0.85V
HIGH	LOW	NA (0.875V)
LOW	HIGH	0.95V
HIGH	HIGH	0.975V

TON1	PR211 = 200K
FREQ	297K

CPU Power



IGPU Power

